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Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CY9B120J Series

32-bit ARM® Cortex®-M3 FM3 Microcontroller

The CY9B120J Series are highly integrated 32-bit microcontrollers dedicated for embedded controllers with low-power consumption mode and competitive cost.

These series are based on the ARM® Cortex®-M3 Processor with on-chip Flash memory and SRAM, and have peripheral functions such as various timers, ADCs and Communication Interfaces (UART, CSIO, I²C, LIN).

The products which are described in this data sheet are placed into TYPE10 product categories in FM3 Family Peripheral Manual.

Features

32-bit ARM® Cortex®-M3 Core

- Processor version: r2p1
- Up to 72 MHz Frequency Operation
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-chip Memories

[Flash memory]

- 64 Kbytes
- Read cycle: 0 wait-cycle
- Security function for code protection

[SRAM]

This Series on-chip SRAM is composed of two independent SRAM (SRAM0, SRAM1). SRAM0 is connected to I-code bus and D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

- SRAM0: 4 Kbytes
- SRAM1: 4 Kbytes

Multi-function Serial Interface (Max four channels)

- 2 channels with 16steps×9-bit FIFO (ch.0/ch.1), 2 channels without FIFO (ch.2/ ch.5)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - I²C

[UART]

- Full-duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Various error detection functions available (parity errors, framing errors, and overrun errors)

[CSIO]

- Full-duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detection function available

[LIN]

- LIN protocol Rev.2.1 supported
- Full-duplex double buffer
- Master/Slave mode supported
- LIN break field generate (can be changed 13-bit to 16-bit length)
- LIN break delimiter generate (can be changed 1-bit to 4-bit length)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

[I²C]

Standard-mode (Max 100 kbps) / Fast-mode (Max 400kbps) supported

DMA Controller (Four channels)

The DMA Controller has an independent bus from the CPU, so CPU and DMA Controller can process simultaneously.

- 4 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: byte/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

A/D Converter (Max 8channels)

[12-bit A/D Converter]

- Successive Approximation type
- Conversion time: 1.0 µs @ 5 V
- Priority conversion available (priority at 2 levels)
  Not included the function to activate A/D by external trigger input
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4steps)

Base Timer (Max eight channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General-Purpose I/O Port

This series can use its pins as general-purpose I/O ports when they are not used for peripherals. Moreover, the port relocate function is built-in. It can set which I/O port the peripheral function can be allocated to.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 23 fast general-purpose I/O Ports@32pin Package
- Some ports are 5V tolerant

  See List of Pin Functions and I/O Circuit Type to confirm the corresponding pins.

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Quadrature Position/Revolution Counter (QPRC) (One channel)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use as the up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Multi-function Timer

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3ch.
- Input capture × 4ch.
- Output compare × 6ch.
- A/D activation compare × 1ch.
- Waveform generator × 3ch.
- 16-bit PPG timer × 3ch.

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

Real-time clock (RTC)

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

- The interrupt function with specifying date and time (Year/Month/Day/Hour/Minute) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

External Interrupt Controller Unit

- Up to 7 external interrupt input pins@32 pin Package
- Include one non-maskable interrupt (NMI) input pin

Watchdog Timer (Two channels)
A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a Hardware watchdog and a Software watchdog.

The "Hardware" watchdog timer is clocked by the built-in Low-speed CR oscillator. Therefore, the "Hardware" watchdog is active in any low-power consumption modes except RTC, Stop modes.

Clock and Reset

[Clocks]
Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillator, and Main PLL).

- Main Clock: 4 MHz to 48 MHz
- Sub Clock: 32.768 kHz
- Built-in High-speed CR Clock: 4 MHz
- Built-in Low-speed CR Clock: 100 kHz
- Main PLL Clock

[Resets]
- Reset requests from INITX pin
- Power on reset
- Software reset
- Watchdog timers reset
- Low-Voltage detection reset
- Clock Super Visor reset

Clock Super Visor (CSV)
Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

- If external clock failure (clock stop) is detected, reset is asserted.
- If external frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Consumption Detector (LVD)
This Series includes 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage that has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-Power Consumption Mode
Four low-power consumption modes supported.

- Sleep
- Timer
- RTC
- Stop

Debug
Serial Wire Debug Port (SW-DP)

Unique ID
Unique value of the device (41-bit) is set.

Power Supply
Wide range voltage: VCC = 2.7 V to 5.5 V

Contents

1. Product Lineup

Memory Size

Product name		CY9BF121J
On-chip Flash memory		64 Kbytes
On-chip SRAM	SRAM0	4 Kbytes
	SRAM1	4 Kbytes
	Total	8 Kbytes

Function

Product name			CY9BF121J
Pin count			32
CPU			Cortex-M3
	Freq.		72 MHz
Power supply voltage range			2.7 V to 5.5 V
DMAC			4 ch.
Multi-function Serial Interface (UART/CSIO/I^{2}C)			4 ch. (Max) ch.0/ch.1: FIFO ch.2/ch.5: No FIFO
Base Timer (PWC/Reload timer/PWM/PPG)			8ch. (Max)
MF-Timer	A/D activation compare	1 ch.	1 unit
	Input capture	4 ch.	
	Free-run timer	3 ch.	
	Output compare	6 ch.	
	Waveform generator	3 ch.	
	PPG	3 ch.	
QPRC			1 ch.
Dual Timer			1 unit
Real-Time Clock			1 unit
Watchdog timer			1 ch. (SW) + 1 ch. (HW)
External Interrupts			7 pins (Max) + NMI × 1
I/O ports			23 pins (Max)
12-bit A/D converter			8 ch. (1 unit)
CSV (Clock Super Visor)			Yes
LVD (Low-Voltage Detector)			2 ch.
Built-in CR	High-speed		4 MHz
	Low-speed		100 kHz
Debug Function			SW-DP
Unique ID			Yes

Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use. See Electrical Characteristics, AC Characteristics, Built-in CR Oscillation Characteristics for accuracy of built-in CR.*

2. Packages

Package \ Product name	CY9BF121J
LQFP: LQB032 (0.8 mm pitch)	❍
QFN: WNU032 (0.5 mm pitch)	❍

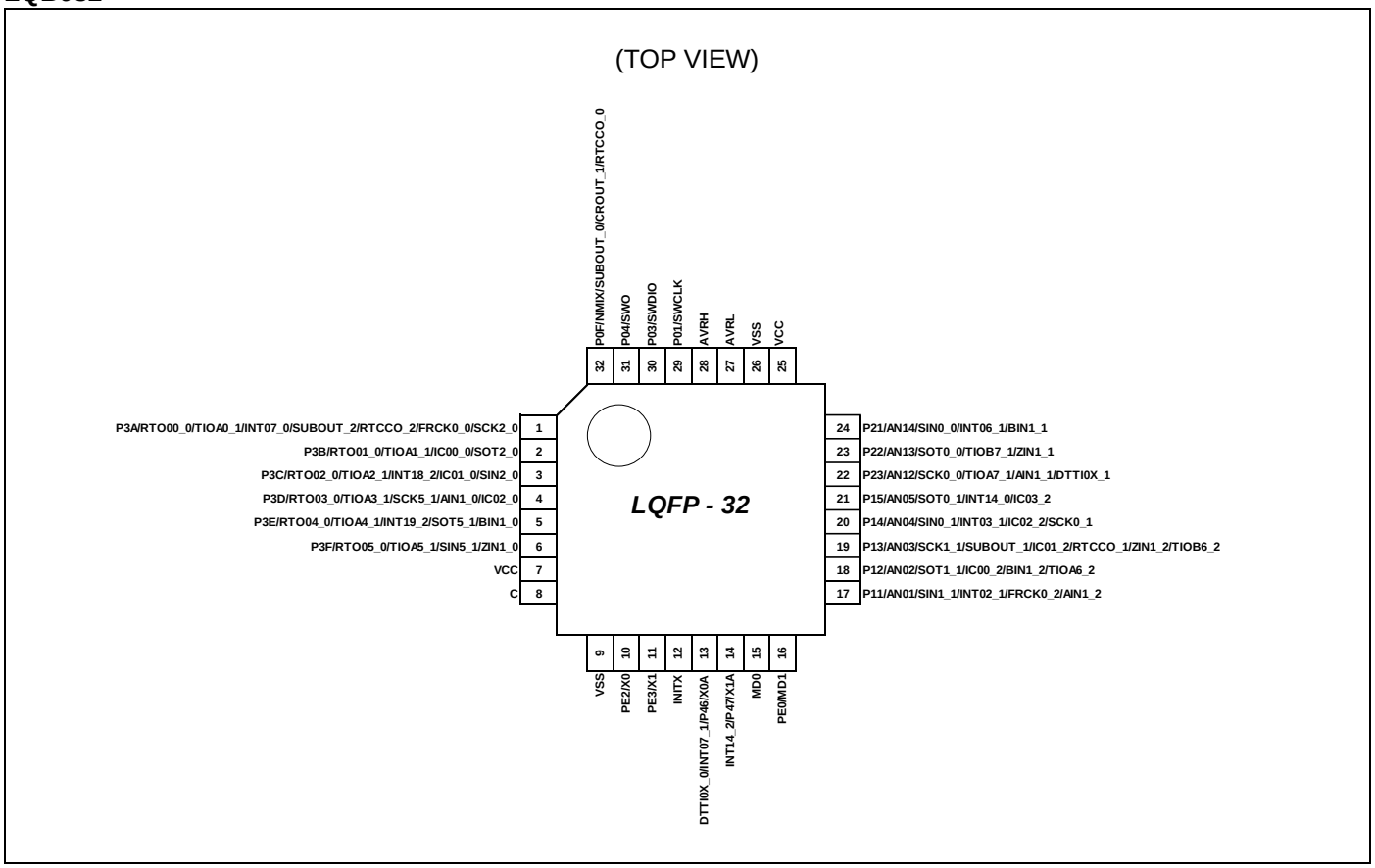
❍: Supported

Note:

- *See Package Dimensions for detailed information on each package.*

3. Pin Assignment

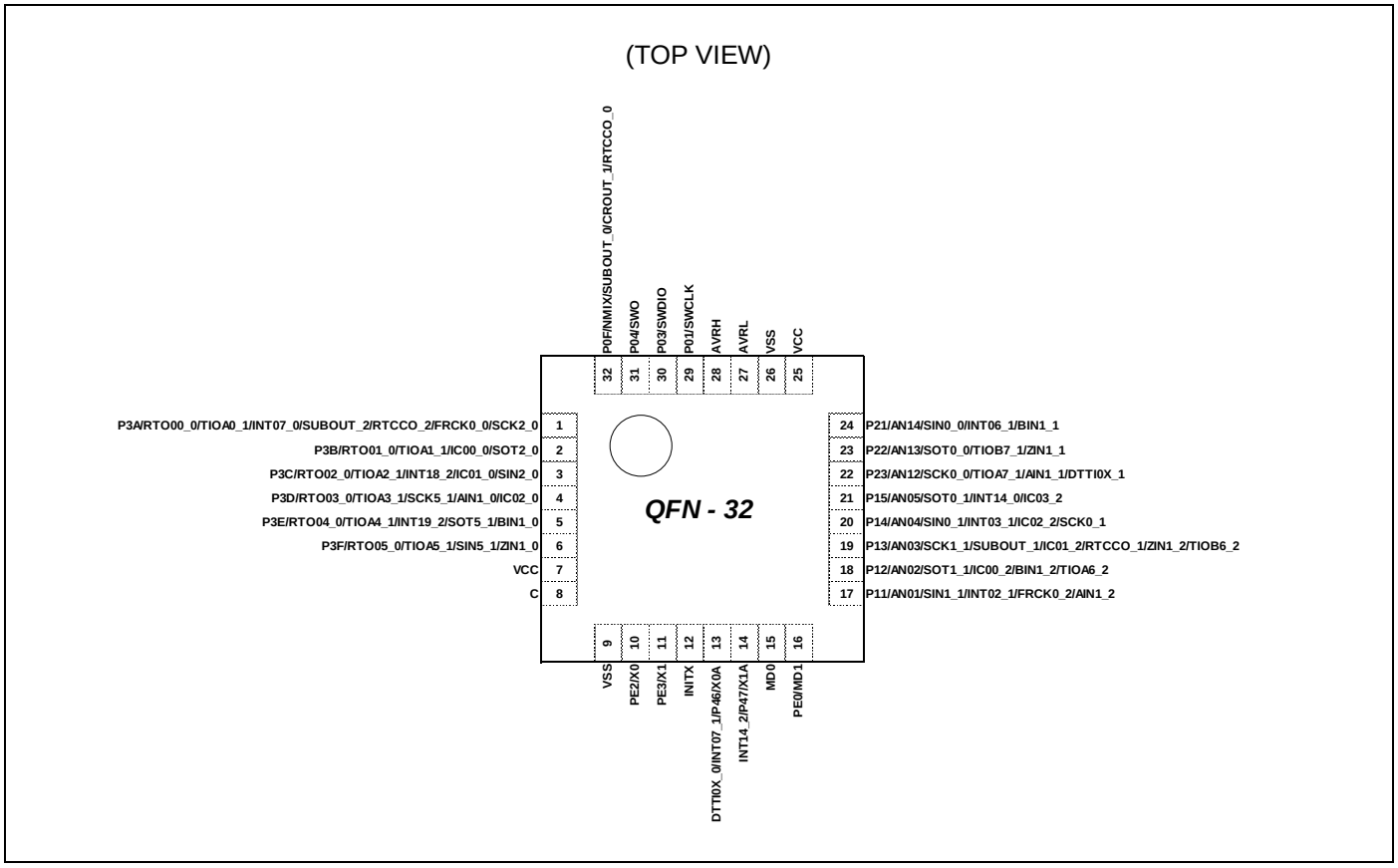
LQB032



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

WNU032



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

4. List of Pin Functions

List of Pin Numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No	Pin name	I/O circuit type	Pin state type
1	P3A	F	K
	RTO00_0 (PPG00_0)		
	FRCK0_0		
	INT07_0		
	TIOA0_1		
	SCK2_0 (SCL2_0)		
	SUBOUT_2		
	RTCCO_2		
2	P3B	F	J
	RTO01_0 (PPG00_0)		
	IC00_0		
	TIOA1_1		
	SOT2_0 (SDA2_0)		
3	P3C	F	K
	RTO02_0 (PPG02_0)		
	IC01_0		
	INT18_2		
	TIOA2_1		
	SIN2_0		
4	P3D	F	J
	RTO03_0 (PPG02_0)		
	IC02_0		
	TIOA3_1		
	SCK5_1 (SCL5_1)		
	AIN1_0		
5	P3E	F	K
	RTO04_0 (PPG04_0)		
	INT19_2		
	TIOA4_1		
	SOT5_1 (SDA5_1)		
	BIN1_0		

Pin No	Pin name	I/O circuit type	Pin state type
6	P3F	F	J
	RTO05_0 (PPG04_0)		
	TIOA5_1		
	SIN5_1		
	ZIN1_0		
7	VCC	-	-
8	C	-	-
9	VSS	-	-
10	PE2	A	A
	X0		
11	PE3	A	B
	X1		
12	INITX	B	C
13	P46	D	F
	X0A		
	DTTI0X_0		
	INT07_1		
14	P47	D	G
	X1A		
	INT14_2		
15	MD0	H	D
16	PE0	C	E
	MD1		
17	P11	G*	M
	AN01		
	SIN1_1		
	INT02_1		
	FRCK0_2		
	AIN1_2		
18	P12	G*	L
	AN02		
	SOT1_1 (SDA1_1)		
	TIOA6_2		
	IC00_2		
	BIN1_2		

Pin No	Pin name	I/O circuit type	Pin state type
19	P13	G*	L
	AN03		
	SCK1_1 (SCL1_1)		
	SUBOUT_1		
	TIOB6_2		
	IC01_2		
	RTCCO_1		
	ZIN1_2		
20	P14	G*	M
	AN04		
	SIN0_1		
	INT03_1		
	SCK0_1 (SCL0_1)		
	IC02_2		
21	P15	G*	M
	AN05		
	SOT0_1 (SDA0_1)		
	INT14_0		
	IC03_2		
22	P23	G*	L
	AN12		
	SCK0_0 (SCL0_0)		
	TIOA7_1		
	DTTI0X_1		
	AIN1_1		
23	P22	G*	L
	AN13		
	SOT0_0 (SDA0_0)		
	TIOB7_1		
	ZIN1_1		
24	P21	G*	M
	AN14		
	SIN0_0		
	INT06_1		
	BIN1_1		
25	VCC	-	-
26	VSS	-	-

Pin No	Pin name	I/O circuit type	Pin state type
27	AVRL	-	-
28	AVRH	-	-
29	P01	E	I
	SWCLK		
30	P03	E	I
	SWDIO		
31	P04	E	I
	SWO		
32	P0F	E	H
	NMIX		
	SUBOUT_0		
	CROUT_1		
	RTCCO_0		

*: 5 V tolerant I/O

List of Pin Functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

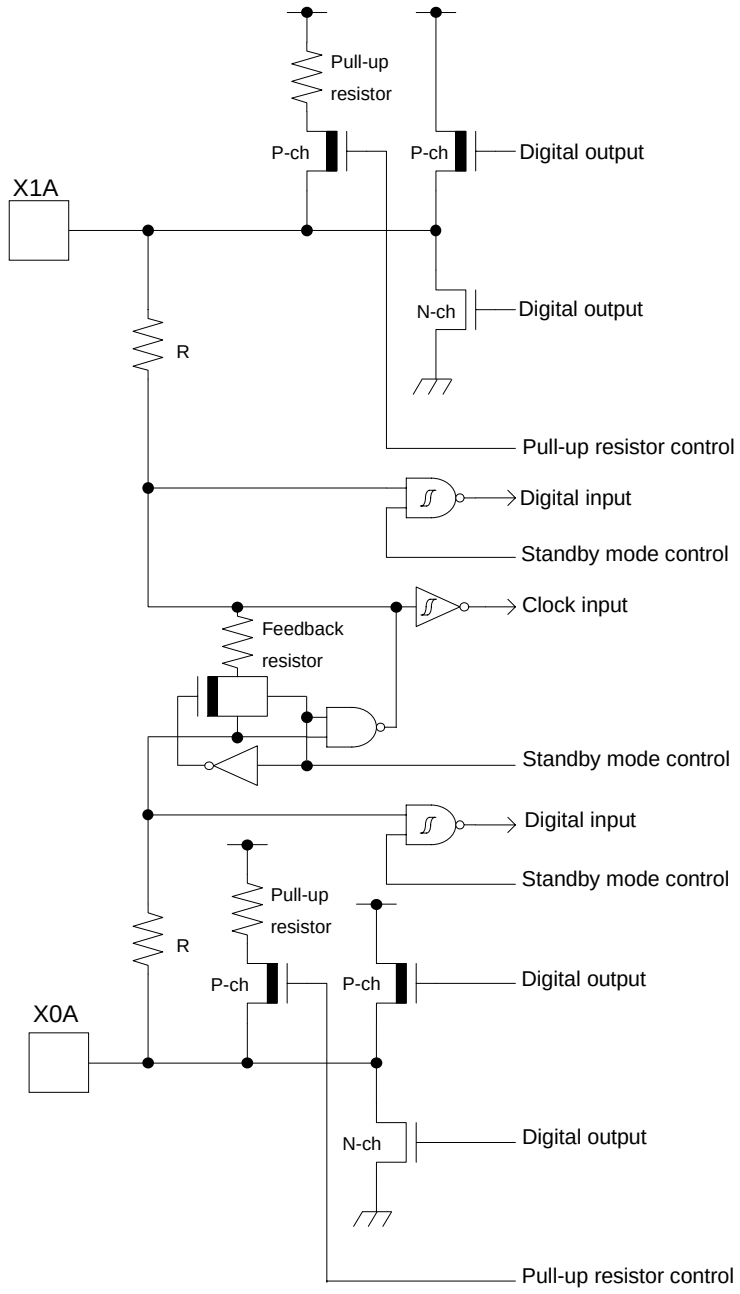
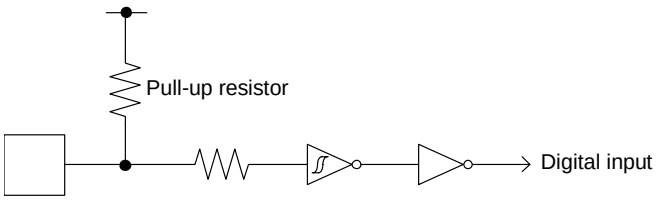
Pin function	Pin name	Function description	Pin No
ADC	AN01	A/D converter analog input pin. ANxx describes ADC ch.xx.	17
	AN02		18
	AN03		19
	AN04		20
	AN05		21
	AN12		22
	AN13		23
	AN14		24
Base Timer 0	TIOA0_1	Base timer ch.0 TIOA pin	1
Base Timer 1	TIOA1_1	Base timer ch.1 TIOA pin	2
Base Timer 2	TIOA2_1	Base timer ch.2 TIOA pin	3
Base Timer 3	TIOA3_1	Base timer ch.3 TIOA pin	4
Base Timer 4	TIOA4_1	Base timer ch.4 TIOA pin	5
Base Timer 5	TIOA5_1	Base timer ch.5 TIOA pin	6
Base Timer 6	TIOA6_2	Base timer ch.6 TIOA pin	18
	TIOB6_2	Base timer ch.6 TIOB pin	19
Base Timer 7	TIOA7_1	Base timer ch.7 TIOA pin	22
	TIOB7_1	Base timer ch.7 TIOB pin	23
Debugger	SWCLK	Serial wire debug interface clock input pin	29
	SWDIO	Serial wire debug interface data input / output pin	30
	SWO	Serial wire viewer output pin	31
External Interrupt	INT02_1	External interrupt request 02 input pin	17
	INT03_1	External interrupt request 03 input pin	20
	INT06_1	External interrupt request 06 input pin	24
	INT07_0	External interrupt request 07 input pin	1
	INT07_1		13
	INT14_0	External interrupt request 14 input pin	21
	INT14-2		14
	INT18_2	External interrupt request 18 input pin	3
	INT19_2	External interrupt request 19 input pin	5
	NMIX	Non-Maskable Interrupt input pin	32

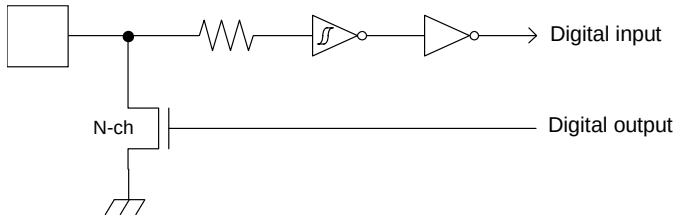
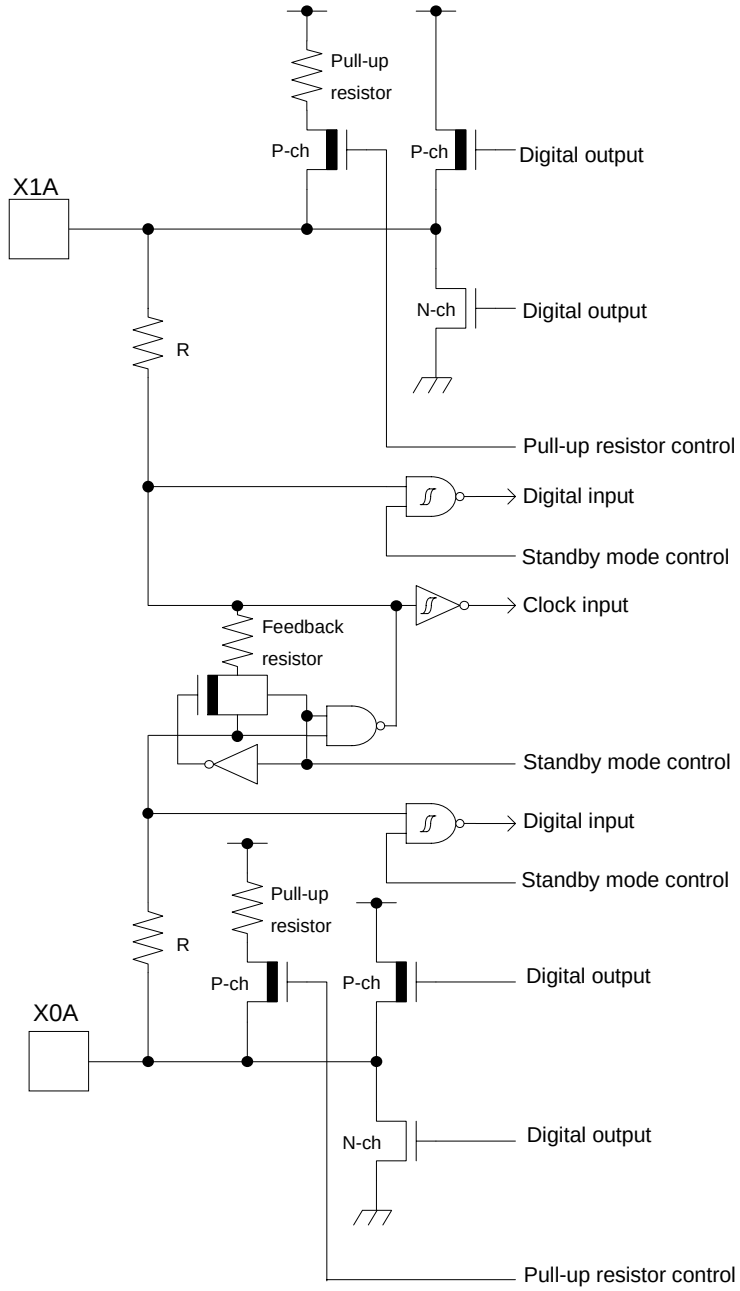
Pin function	Pin name	Function description	Pin No
GPIO	P01	General-purpose I/O port 0	29
	P03		30
	P04		31
	P0F		32
	P11	General-purpose I/O port 1	17
	P12		18
	P13		19
	P14		20
	P15		21
	P21	General-purpose I/O port 2	24
	P22		23
	P23		22
	P3A	General-purpose I/O port 3	1
	P3B		2
	P3C		3
	P3D		4
	P3E		5
	P3F		6
	P46	General-purpose I/O port 4	13
	P47		14
	PE0	General-purpose I/O port E	16
	PE2		10
	PE3		11
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	24
	SIN0_1		20
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I^2C (operation mode 4).	23
	SOT0_1 (SDA0_1)		21
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a CSIO (operation mode 2) and as SCL0 when it is used in an I^2C (operation mode 4).	22
	SCK0_1 (SCL0_1)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a CSIO (operation mode 2) and as SCL0 when it is used in an I^2C (operation mode 4).	20
Multi-function Serial 1	SIN1_1	Multi-function serial interface ch.1 input pin	17
	SOT1_1 (SDA1_1)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I^2C (operation mode 4).	18
	SCK1_1 (SCL1_1)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation mode 2) and as SCL1 when it is used in an I^2C (operation mode 4).	19

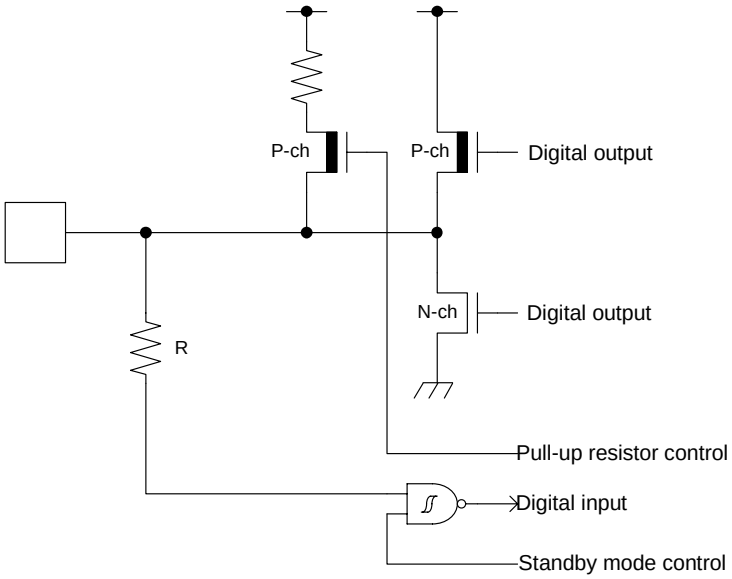
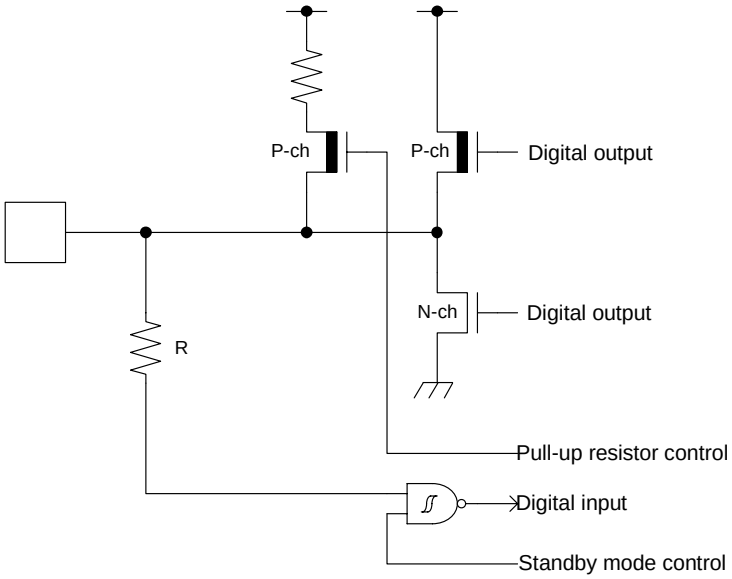
Pin function	Pin name	Function description	Pin No
Multi-function Serial 2	SIN2_0	Multi-function serial interface ch.2 input pin	3
	SOT2_0 (SDA2_0)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I^2C (operation mode 4).	2
	SCK2_0 (SCL2_0)	Multi-function serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a CSIO (operation mode 2) and as SCL2 when it is used in an I^2C (operation mode 4).	1
Multi-function Serial 5	SIN5_1	Multi-function serial interface ch.5 input pin	6
	SOT5_1 (SDA5_1)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I^2C (operation mode 4).	5
	SCK5_1 (SCL5_1)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I^2C (operation mode 4).	4
Multi-function Timer 0	DTTI0X_0	Input signal of waveform generator to control outputs RTO00 to RTO05 of Multi-function timer 0.	13
	DTTI0X_1		22
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin	1
	FRCK0_2		17
	IC00_0	16-bit input capture input pin of Multi-function timer 0. ICxx describes channel number.	2
	IC00_2		18
	IC01_0		3
	IC01_2		19
	IC02_0		4
	IC02_2		20
	IC03_2		21
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	1
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	2
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	3
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	4
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	5
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	6

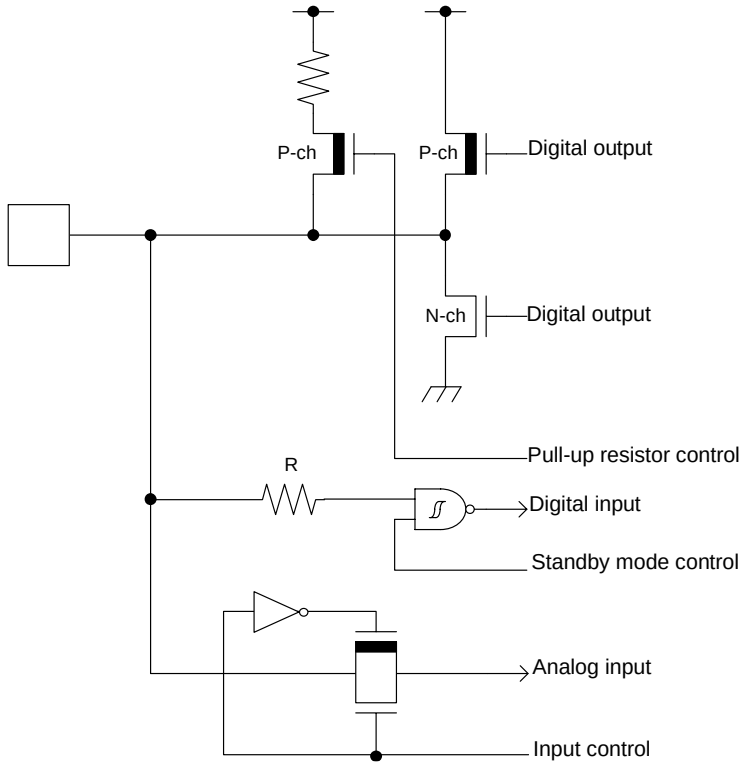
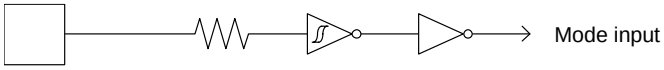
Pin function	Pin name	Function description	Pin No
Quadrature Position/ Revolution Counter	AIN1_0	QPRC ch.1 AIN input pin	4
	AIN1_1		22
	AIN1_2		17
	BIN1_0	QPRC ch.1 BIN input pin	5
	BIN1_1		24
	BIN1_2		18
	ZIN1_0	QPRC ch.1 ZIN input pin	6
	ZIN1_1		23
	ZIN1_2		19
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	32
	RTCCO_1		19
	RTCCO_2		1
	SUBOUT_0	Sub clock output pin	32
	SUBOUT_1		19
	SUBOUT_2		1
RESET	INITX	External Reset Input pin. A reset is valid when INITX="L".	12
Mode	MD0	Mode 0 pin. During normal operation, MD0="L" must be input. During serial programming to Flash memory, MD0="H" must be input.	15
	MD1	Mode 1 pin. During serial programming to Flash memory, MD1="L" must be input.	16
POWER	VCC	Analog/Digital Power supply Pin	7
	VCC	Analog/Digital Power supply Pin	25
GND	VSS	Analog/Digital GND Pin	9
	VSS	Analog/Digital GND Pin	26
CLOCK	X0	Main clock (oscillation) input pin	10
	X0A	Sub clock (oscillation) input pin	13
	X1	Main clock (oscillation) I/O pin	11
	X1A	Sub clock (oscillation) I/O pin	14
	CROUT_1	Built-in High-speed CR-osc clock output port	32
Analog POWER	AVRH	A/D converter analog reference voltage input pin	28
Analog GND	AVRL	A/D converter analog reference voltage input pin	27
C pin	C	Power supply stabilization capacity pin	8

5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. – Oscillation feedback resistor : Approximately 1 MΩ – With standby mode control When the GPIO is selected. – CMOS level output. – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH}= -4 mA, I_{OL}= 4 mA
B		– CMOS level hysteresis input – Pull-up resistor : Approximately 50 kΩ

Type	Circuit	Remarks
C		– Open drain output – CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. – Oscillation feedback resistor : Approximately 5 MΩ – With standby mode control When the GPIO is selected. – CMOS level output. – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH}= -4 mA, I_{OL}= 4 mA

Type	Circuit	Remarks
E		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH}= -4 mA, I_{OL}= 4 mA – +B input is available
F		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH}= -12 mA, I_{OL}= 12 mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off – +B input is available

Type	Circuit	Remarks
G		– CMOS level output – CMOS level hysteresis input – With input control – Analog input – 5 V tolerant – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH}= -4 mA, I_{OL}= 4 mA – Available to control of PZR registers. – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
H		CMOS level hysteresis input

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.
3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason, it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

7. Handling Devices

Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin, between AVRH pin and AVRL pin near this device.

Stabilizing supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply.

Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Sub crystal oscillator

This series sub oscillator circuit is low gain to keep the low current consumption. The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

■Surface mount type

Size:	More than 3.2 mm × 1.5 mm
Load capacitance:	Approximately 6 pF to 7 pF

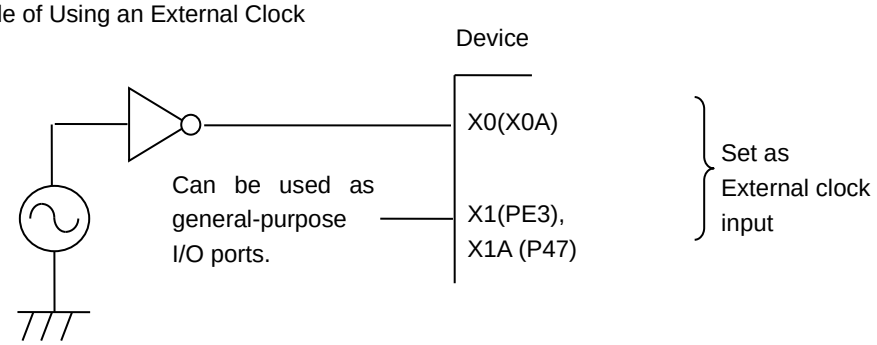
■Lead type

Load capacitance:	Approximately 6 pF to 7 pF

Using an external clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

• Example of Using an External Clock

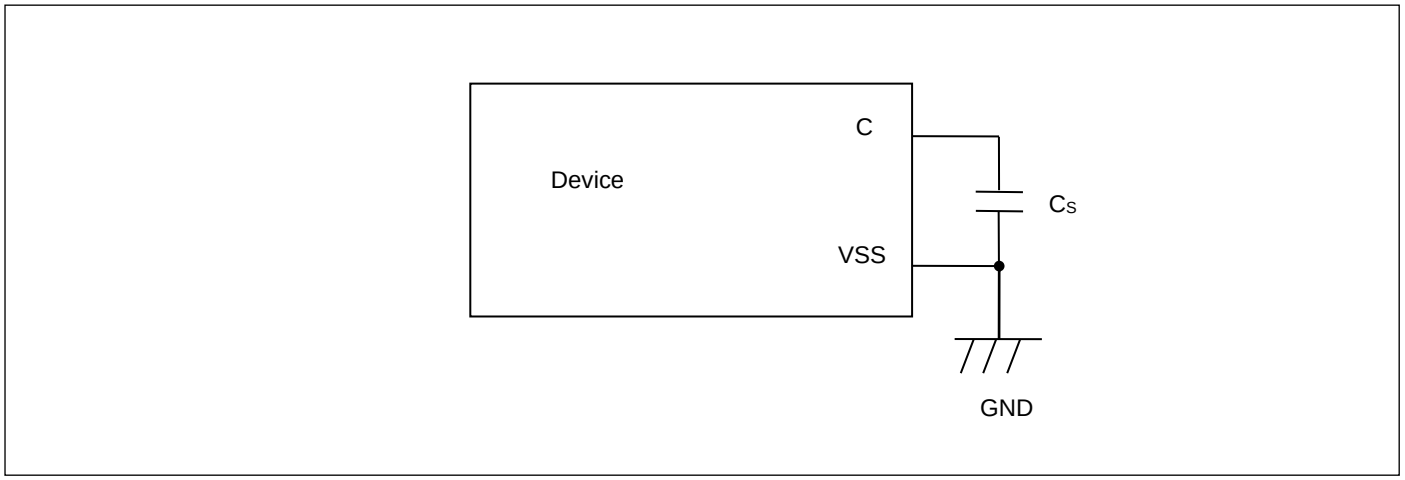


Handling when using Multi-function serial pin as I²C pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7µF would be recommended for this series.



Mode pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Notes on power-on

Turn power on/off in the following order or at the same time.

Turning on: VCC → AVRH

Turning off: AVRH → VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

Differences in features among the products with different memory sizes and between Flash memory products and MASK products

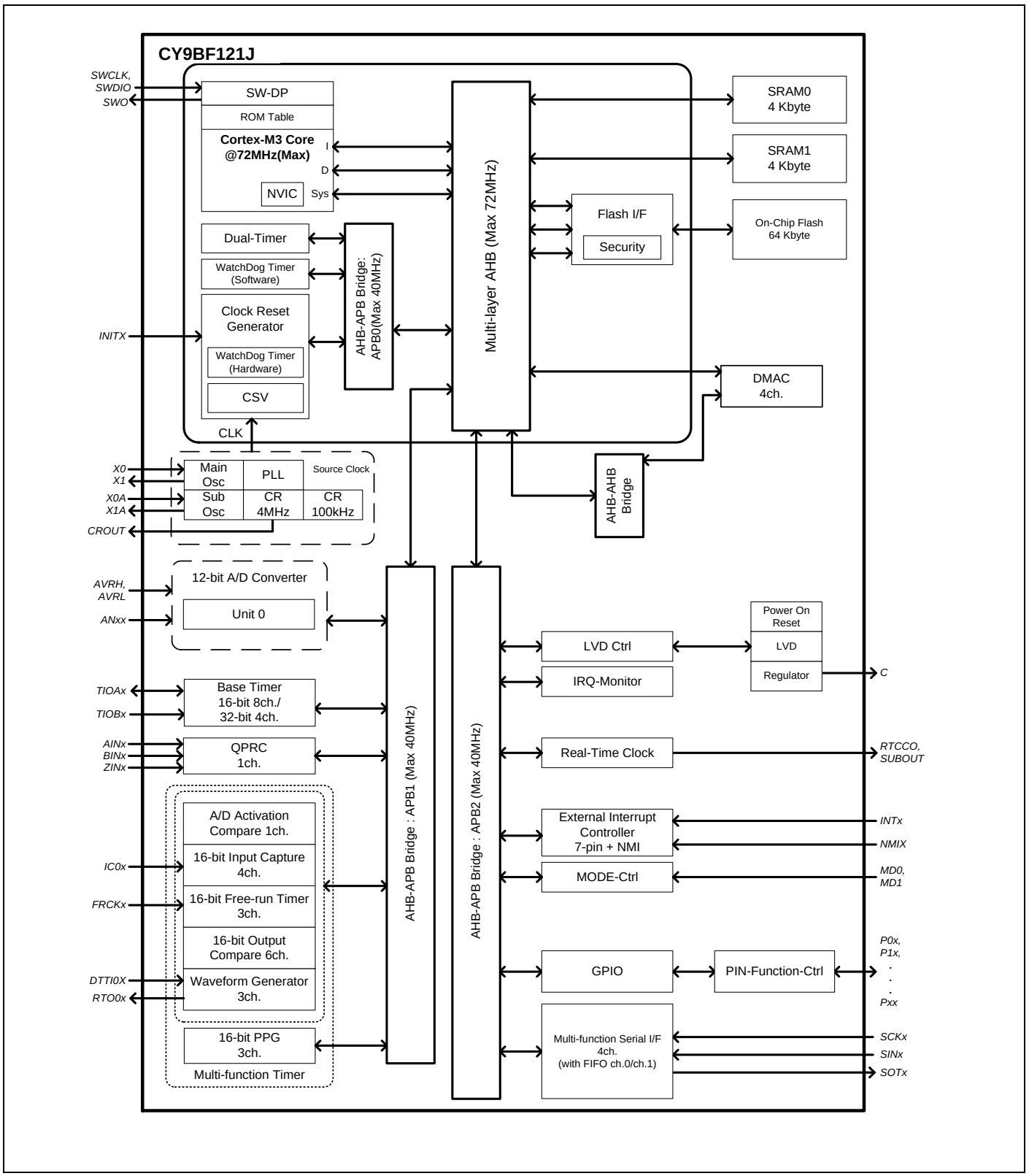
The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up function of 5 V tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

8. Block Diagram

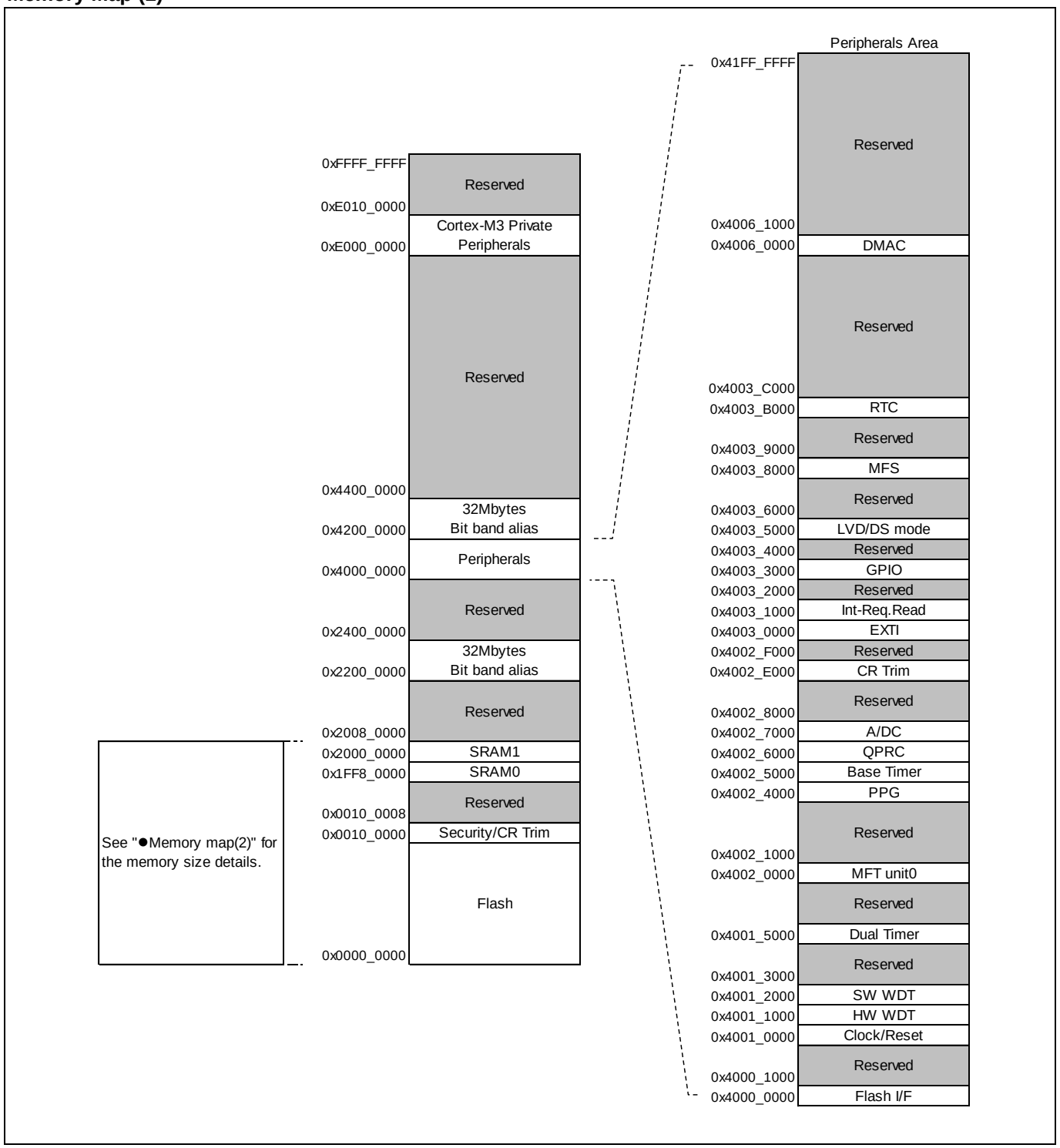


9. Memory Size

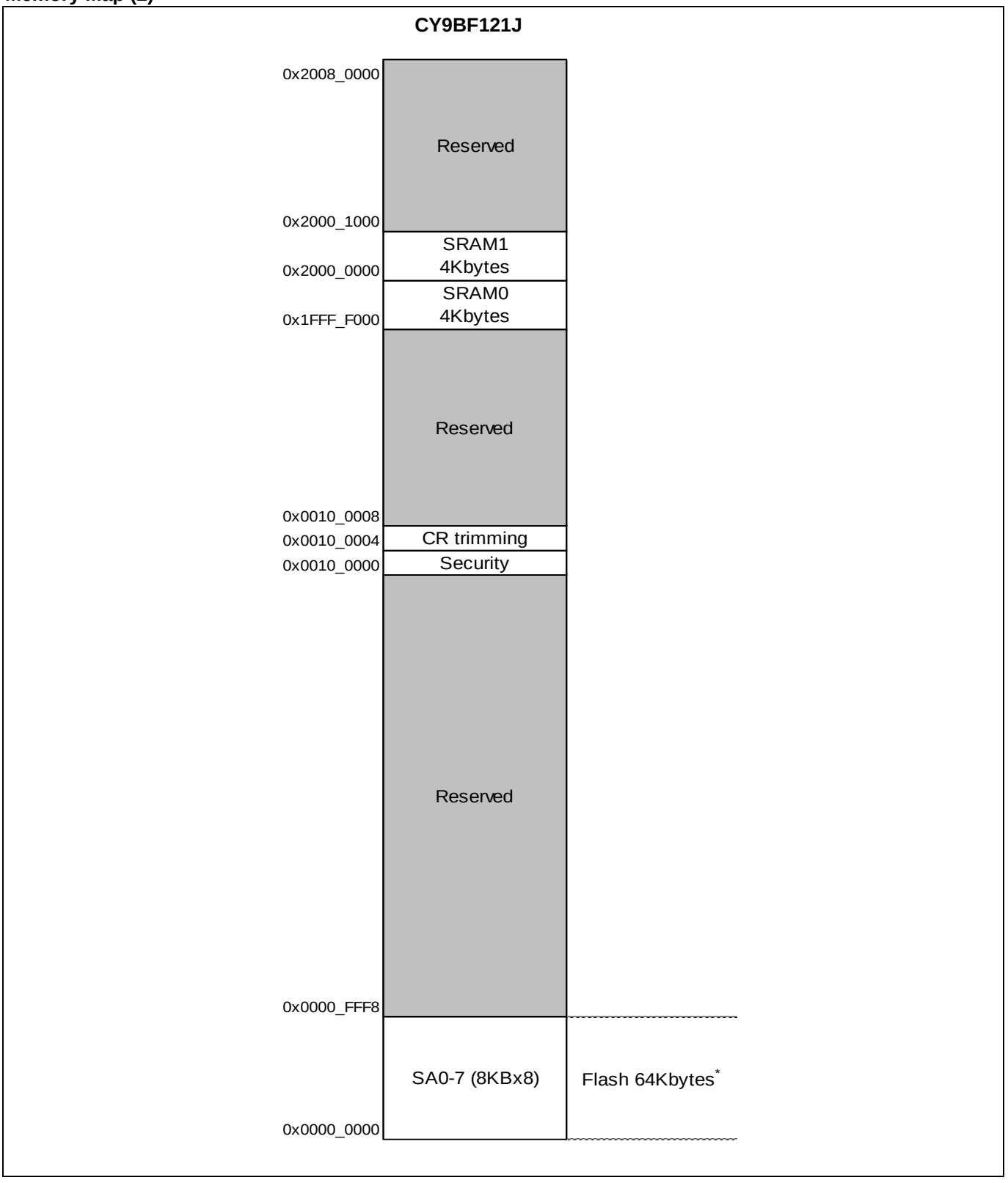
See Memory size in Product Lineup to confirm the memory size.

10. Memory Map

Memory Map (1)



Memory Map (2)



*: See “CY9A420L/120L/CY9B120J SERIES FM3 FLASH PROGRAMMING SPECIFICATIONS” to confirm the detail of Flash memory.

Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Built-in CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low-Voltage Detector
0x4003_5800	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_AFFF		Reserved
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_FFFF		Reserved
0x4004_0000	0x4005_FFFF	AHB	Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x41FF_FFFF		Reserved

11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

- INITX=0

  This is the period when the INITX pin is the L level.

- INITX=1

  This is the period when the INITX pin is the H level.

- SPL=0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

- SPL=1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at 0

  This is the status that the input function cannot be used. Internal input is fixed at L.

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

List of Pin Status

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	TIMER mode, RTC mode or STOP mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	Main crystal oscillator input pin /External main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0
	Main crystal oscillator output pin	Hi-Z / Internal input fixed at 0 or Input enable	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z / Internal input fixed at 0
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	TIMER mode, RTC mode or STOP mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Input enabled
F	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Sub crystal oscillator input pin /External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
G	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0
	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at 0 or Input enable	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at 0

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	TIMER mode, RTC mode or STOP mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1
H	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0
	GPIO selected						
I	Serial wire debug selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0
J	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0
	GPIO selected						
K	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0
	GPIO selected						
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0
	GPIO selected						

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	TIMER mode, RTC mode or STOP mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1
M	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected						Hi-Z / Internal input fixed at 0
	GPIO selected						

*1: Oscillation is stopped at Sub Timer mode, Low-speed CR Timer mode, RTC mode, Stop mode.

*2: Oscillation is stopped at Stop mode.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage*1, *3	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage*1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage*1	V_{IA}	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage*1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
Clamp maximum current	I_{CLAMP}	-2	+2	mA	*7
Clamp total maximum current	$\Sigma[I_{CLAMP}]$		+20	mA	*7
L level maximum output current*4	I_{OL}	-	10	mA	4 mA type
			20	mA	12 mA type
L level average output current*5	I_{OLAV}	-	4	mA	4 mA type
			12	mA	12 mA type
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current*6	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current*4	I_{OH}	-	- 10	mA	4 mA type
			- 20	mA	12 mA type
H level average output current*5	I_{OHAV}	-	- 4	mA	4 mA type
			- 12	mA	12 mA type
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current*6	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	350	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that V_{SS} = 0 V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: Ensure that the voltage does not to exceed V_{CC} + 0.5 V, for example, when the power is turned on.

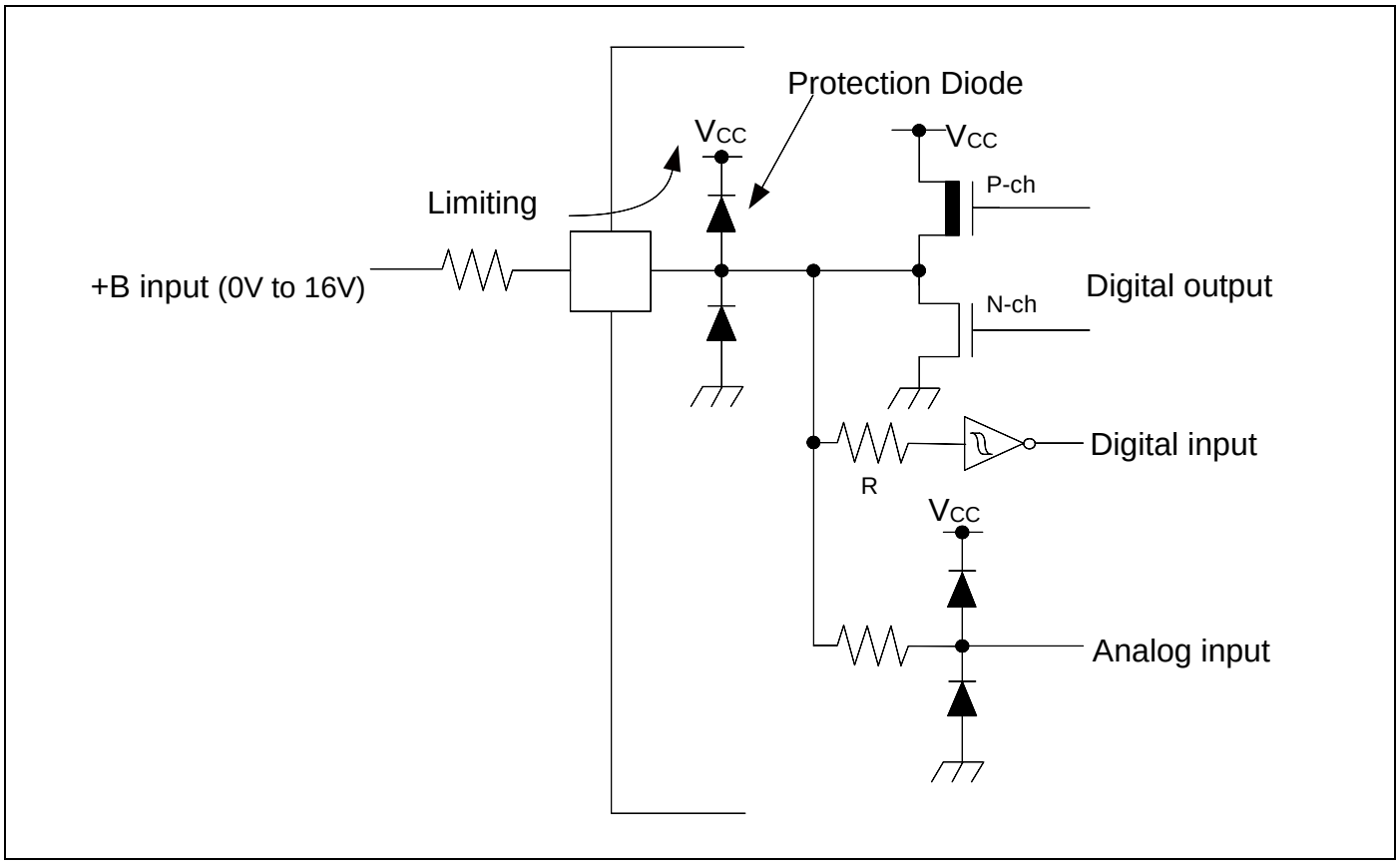
*4: The maximum output current is the peak value for a single pin.

*5: The average output is the average current for a single pin over a period of 100 ms.

*6: The total average output current is the average current for all pins over a period of 100 ms.

*7:

- See List of Pin Functions and I/O Circuit Type about +B input available pin.
- Use within recommended operating conditions.
- Use at DC voltage (current) the +B input.
- The +B signal should always be applied a limiting resistance placed between the +B signal and the device.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the device pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the device drive current is low, such as in the low-power consumption modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the device power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- The following is a recommended circuit example (I/O equivalent circuit).



WARNING:

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.*
  Do not exceed any of these ratings.

12.2 Recommended Operating Conditions

(V_{SS} = AVRL = 0.0V)

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		V_{CC}	-	2.7*2	5.5	V	
Analog reference voltage		AVRH	-	2.7	V_{CC}	V	
		AVRL	-	V_{SS}	V_{SS}	V	
Smoothing capacitor		C_S	-	1	10	µF	For regulator*1
Operating temperature	LQB032, WNU032	T_A	When mounted on four-layer PCB	- 40	+ 105	°C	
			When mounted on double-sided single-layer PCB	- 40	+ 85	°C	

*1: See C Pin in Handling Devices for the connection of the smoothing capacitor.

*2: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate only.

WARNING:

- *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
  Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

12.3 DC Characteristics

12.3.1 Current Rating

(V_{CC} = 2.7V to 5.5V, V_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ	Max		
Run mode current	I_{CC}	VCC	PLL Run mode	CPU: 72 MHz, Peripheral: 36 MHz Instruction on Flash	27	35	mA	*1, *5
				CPU: 72 MHz, Peripheral: the clock stops NOP operation Instruction on Flash	18	22	mA	*1, *5
				CPU: 72 MHz, Peripheral: 36 MHz Instruction on RAM	23	29	mA	*1
			High-speed CR Run mode	CPU/ Peripheral: 4 MHz*2 Instruction on Flash	2.2	3.1	mA	*1
			Sub Run mode	CPU/ Peripheral: 32 kHz Instruction on Flash	73	910	µA	*1, *6
			Low-speed CR Run mode	CPU/ Peripheral: 100k Hz Instruction on Flash	105	930	µA	*1
Sleep mode current	I_{CCS}		PLL Sleep mode	Peripheral: 36 MHz	17	20	mA	*1, *5
			High-speed CR Sleep mode	Peripheral: 4 MHz*2	1.3	2.2	mA	*1
			Sub Sleep mode	Peripheral: 32 kHz	64	890	µA	*1, *6
			Low-speed CR Sleep mode	Peripheral: 100 kHz	80	910	µA	*1

*1: When all ports are fixed.

*2: When setting it to 4 MHz by trimming.

*3: T_A = +25°C, V_{CC} = 5.5 V

*4: T_A = +105°C, V_{CC} = 5.5 V

*5: When using the crystal oscillator of 4 MHz (Including the current consumption of the oscillation circuit)

*6: When using the crystal oscillator of 32 kHz (Including the current consumption of the oscillation circuit)

(V_{CC} = 2.7V to 5.5V, V_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions		Value Typ	Value Max	Unit	Remarks
Timer mode current	I_{CCT}	VCC	Main Timer mode	T_A = + 25°C, When LVD is off	3.5	4.1	mA	*1
				T_A = + 105°C, When LVD is off	-	4.6	mA	*1
	I_{CCT}		Sub Timer mode	T_A = + 25°C, When LVD is off	15	45	µA	*1
				T_A = + 105°C, When LVD is off	-	740	µA	*1
RTC mode current	I_{CCR}		RTC mode	T_A = + 25°C, When LVD is off	13	39	µA	*1
				T_A = + 105°C, When LVD is off	-	580	µA	*1
Stop mode current	I_{CCH}		Stop mode	T_A = + 25°C, When LVD is off	12	33	µA	*1
				T_A = + 105°C, When LVD is off	-	550	µA	*1

*1: When all ports are fixed.

*2: V_{CC} = 5.5 V

*3: When using the crystal oscillator of 4 MHz (Including the current consumption of the oscillation circuit)

*4: When using the crystal oscillator of 32 kHz (Including the current consumption of the oscillation circuit)

LVD current

(V_{CC} = 2.7V to 5.5V, V_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value Typ	Value Max	Unit	Remarks
Low-Voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation for reset V_{CC} = 5.5 V	0.13	0.3	µA	At not detect
			At operation for interrupt V_{CC} = 5.5 V	0.13	0.3	µA	At not detect

Flash memory current

(V_{CC} = 2.7V to 5.5V, V_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value Typ	Value Max	Unit	Remarks
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	9.5	11.2	mA	

A/D convertor current

(V_{CC} = 2.7V to 5.5V, V_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value Typ	Value Max	Unit	Remarks
Power supply current	I_{CCAD}	VCC	At operation	0.7	0.9	mA	
Reference power supply current	I_{CCAVRH}	AVRH	At operation AVRH = 5.5 V	1.1	1.97	mA	
			At stop AVRH = 5.5 V	0.1	1.7	µA	

12.3.2 Pin Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	
		5 V tolerant input pin	-	V_{CC} × 0.8	-	V_{SS} + 5.5	V	
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
		5 V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
H level output voltage	V_{OH}	4 mA type	$V_{CC} \geq 4.5$ V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			$V_{CC} < 4.5$ V, I_{OH} = - 2 mA					
		12 mA type	$V_{CC} \geq 4.5$ V, I_{OH} = - 12 mA	V_{CC} - 0.5	-	V_{CC}	V	
			$V_{CC} < 4.5$ V, I_{OH} = - 8 mA					
L level output voltage	V_{OL}	4 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 2 mA					
		12 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 12 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 8 mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistance value	R_{PU}	Pull-up pin	$V_{CC} \geq 4.5$ V	33	50	90	kΩ	
			$V_{CC} < 4.5$ V	-	-	180		
Input capacitance	C_{IN}	Other than VCC, VSS, AVRH, AVRL	-	-	5	15	pF	

12.4 AC Characteristics

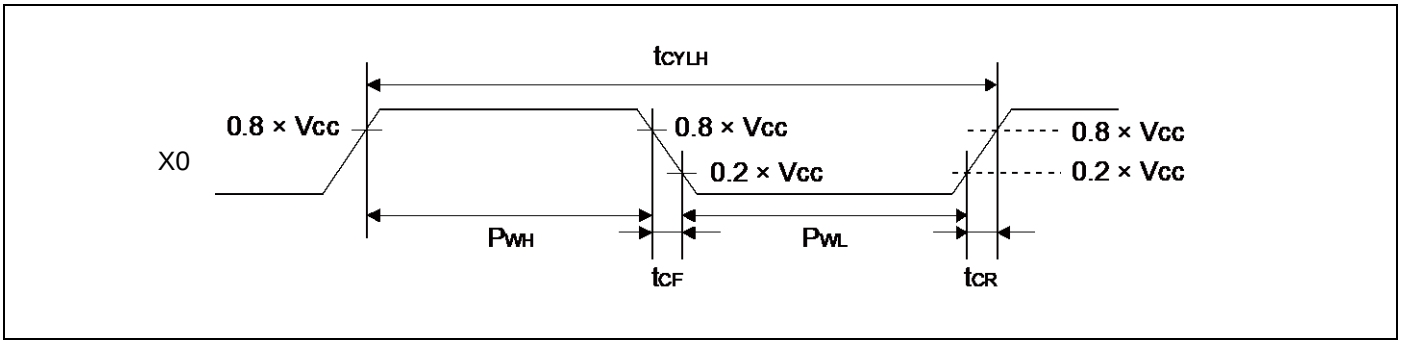
12.4.1 Main Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	$V_{CC} \geq 4.5$ V	4	48	MHz	When crystal oscillator is connected
			$V_{CC} < 4.5$ V	4	20		
			-	4	48	MHz	When using external Clock
Input clock cycle	t_{CYLH}		-	20.83	250	ns	When using external Clock
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external Clock
Input clock rise time and fall time	t_{CF}, t_{CR}		-	-	5	ns	When using external Clock
Internal operating clock*1 frequency	f_{CM}	-	-	-	72	MHz	Master clock
	f_{CC}	-	-	-	72	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	40	MHz	APB0 bus clock*2
	f_{CP1}	-	-	-	40	MHz	APB1 bus clock*2
	f_{CP2}	-	-	-	40	MHz	APB2 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	13.8	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	25	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	25	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	25	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

*2: For about each APB bus which each peripheral is connected to, see Block Diagram in this data sheet.

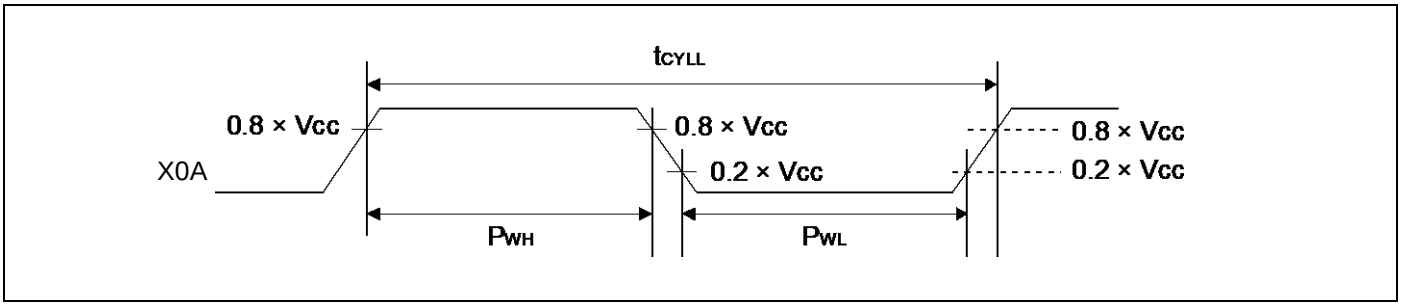


12.4.2 Sub Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected*
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock

*: See Sub crystal oscillator in Handling Devices for the crystal oscillator used.



12.4.3 Built-in CR Oscillation Characteristics

Built-in High-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	T_A = + 25°C, 3.6 V < V_{CC} ≤ 5.5 V	3.92	4	4.08	MHz	When trimming*1
		T_A =0°C to + 85°C, 3.6 V < V_{CC} ≤ 5.5 V	3.9	4	4.1		
		T_A = - 40°C to + 105°C, 3.6 V < V_{CC} ≤ 5.5 V	3.88	4	4.12		
		T_A = + 25°C, 2.7 V ≤ V_{CC} ≤ 3.6 V	3.94	4	4.06		
		T_A = - 20°C to + 85°C, 2.7 V ≤ V_{CC} ≤ 3.6 V	3.92	4	4.08		
		T_A = - 20°C to + 105°C, 2.7 V ≤ V_{CC} ≤ 3.6 V	3.9	4	4.1		
		T_A = - 40°C to + 105°C, 2.7 V ≤ V_{CC} ≤ 3.6 V	3.88	4	4.12		
		T_A = - 40°C to + 105°C	2.8	4	5.2		When not trimming
Frequency stabilization time	t_{CRWT}	-	-	-	30	µs	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming/temperature trimming.

*2: This is time from the trim value setting to stable of the frequency of the High-speed CR clock.
After setting the trim value, the period when the frequency stability time passes can use the High-speed CR clock as a source clock.

Built-in Low-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

12.4.4 Operating Conditions of Main PLL (In the case of using main clock for input of Main PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiple rate	-	5	-	37	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	72	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

12.4.5 Operating Conditions of Main PLL (In the case of using built-in High-speed CR for input clock of Main PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiple rate	-	19	-	35	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	72	-	150	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	72	MHz	

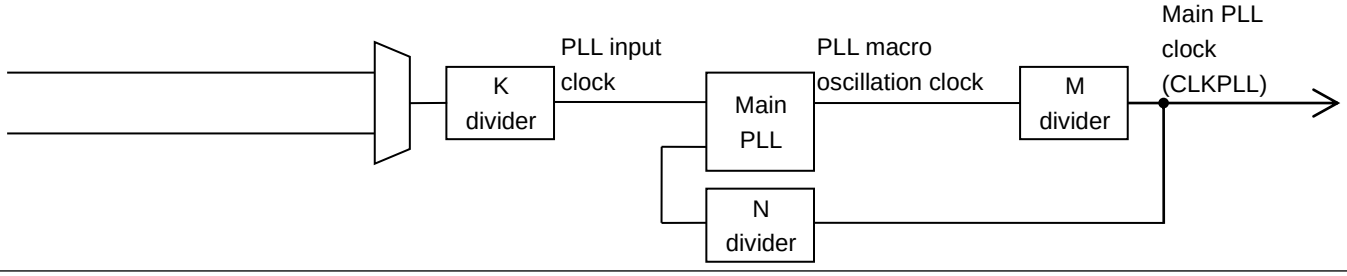
*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

Note:

- *Make sure to input to the Main PLL source clock, the High-speed CR clock (CLKHC) that the frequency/temperature has been trimmed.*
  When setting PLL multiple rate, please take the accuracy of the built-in High-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.

Main PLL connection



12.4.6 Reset Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

12.4.7 Power-on Reset Timing

(V_{SS} = 0V, T_A = - 40°C to + 105°C)

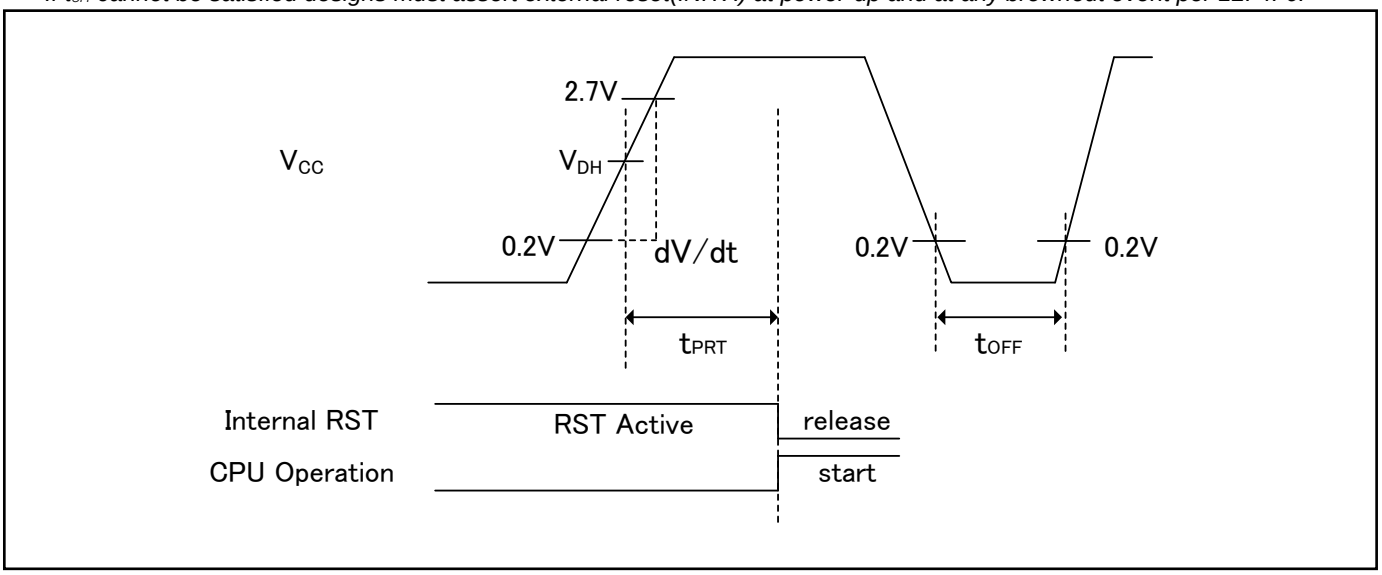
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply shut down time	t_{OFF}	VCC	-	1	-	-	ms	*1
Power ramp rate	dV/dt		Vcc:0.2 V to 2.70 V	1.2	-	1000	mV/µs	*2
Time until releasing Power-on reset	t_{PRT}		-	0.34	-	3.15	ms	

*1: V_{CC} must be held below 0.2 V for minimum period of t_{OFF}. Improper initialization may occur if this condition is not met.

*2: This dV/dt characteristic is applied at the power-on of cold start (t_{OFF}>1 ms).

Note:

- *If t_{OFF} cannot be satisfied designs must assert external reset(INITX) at power-up and at any brownout event per 12. 4. 6.*



Glossary

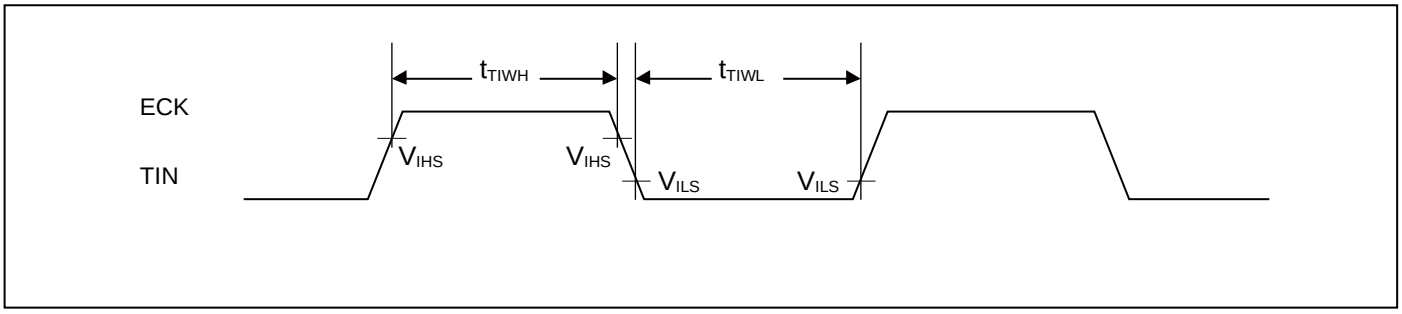
VDH: detection voltage of Low Voltage detection reset. See “12.6. Low-voltage Detection Characteristics”

12.4.8 Base Timer Input Timing

Timer input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

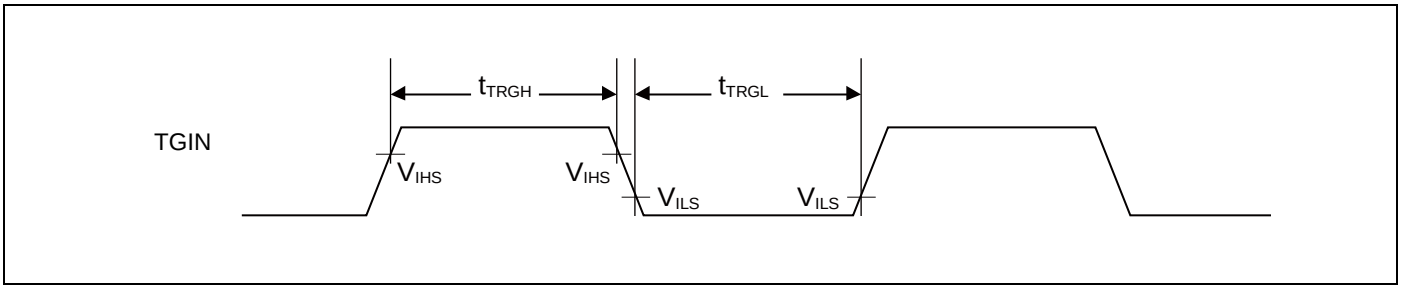
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



Trigger input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Base Timer is connected to, see Block Diagram in this data sheet.

12.4.9 CSIO/UART Timing

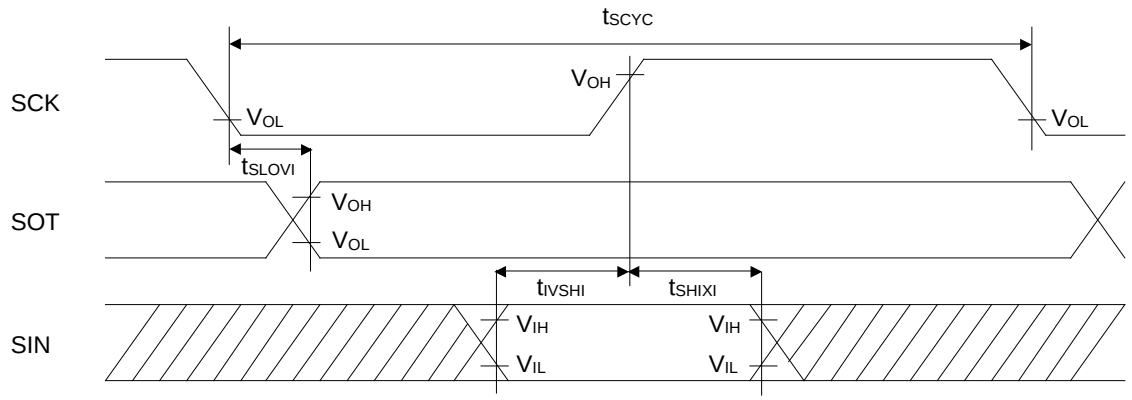
CSIO (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

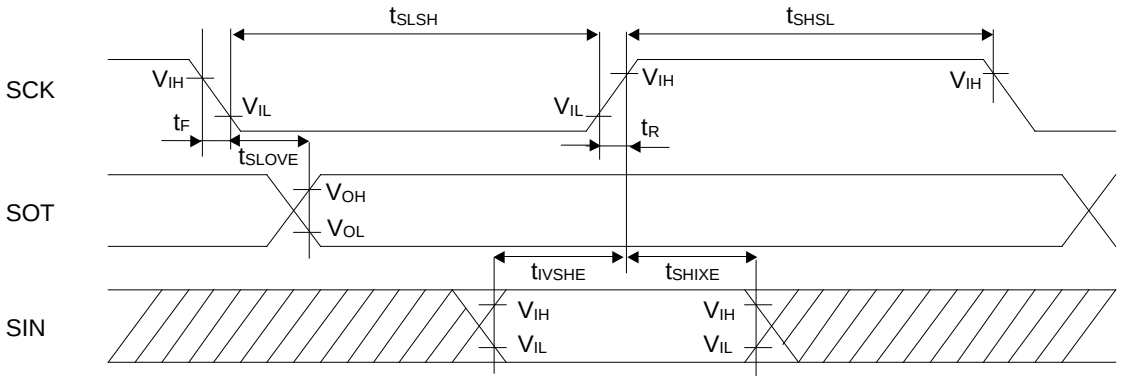
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to clock synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function Serial is connected to, see Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
- *For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*



Master mode



Slave mode

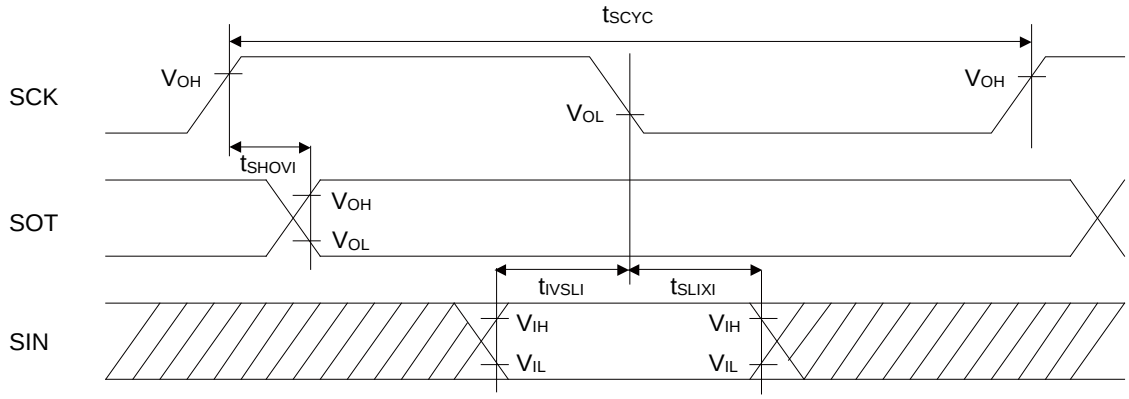
CSIO (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

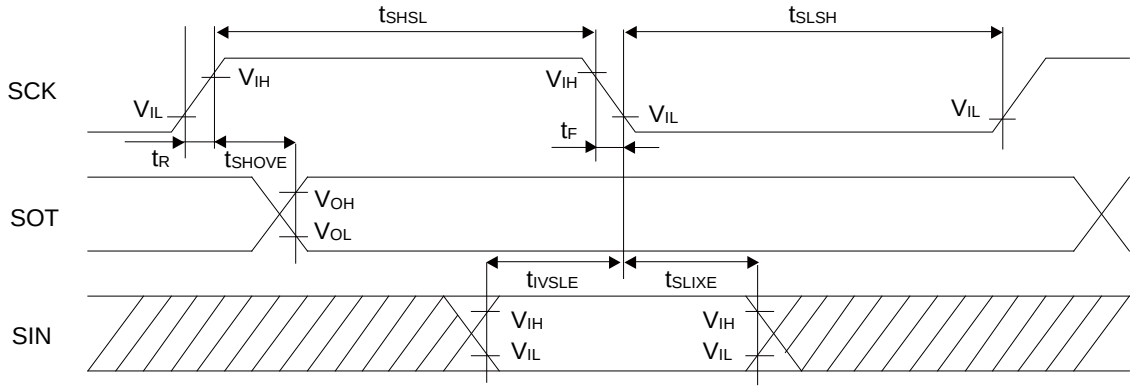
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to clock synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function Serial is connected to, see Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
- *For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*



Master mode



Slave mode

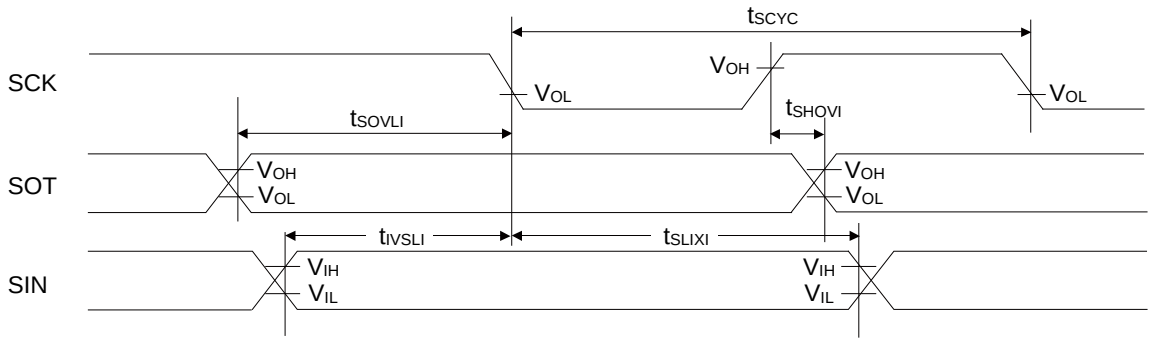
CSIO (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

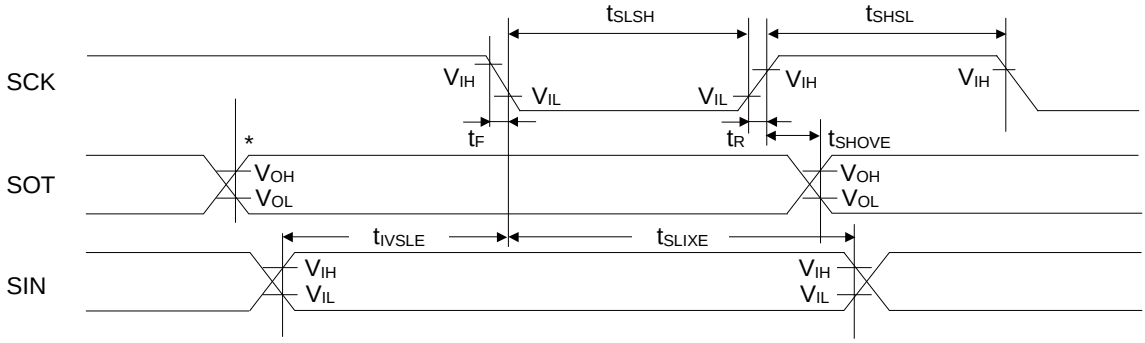
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to clock synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function Serial is connected to, see Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
- *For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*



Master mode



Slave mode

*: Changes when writing to TDR register

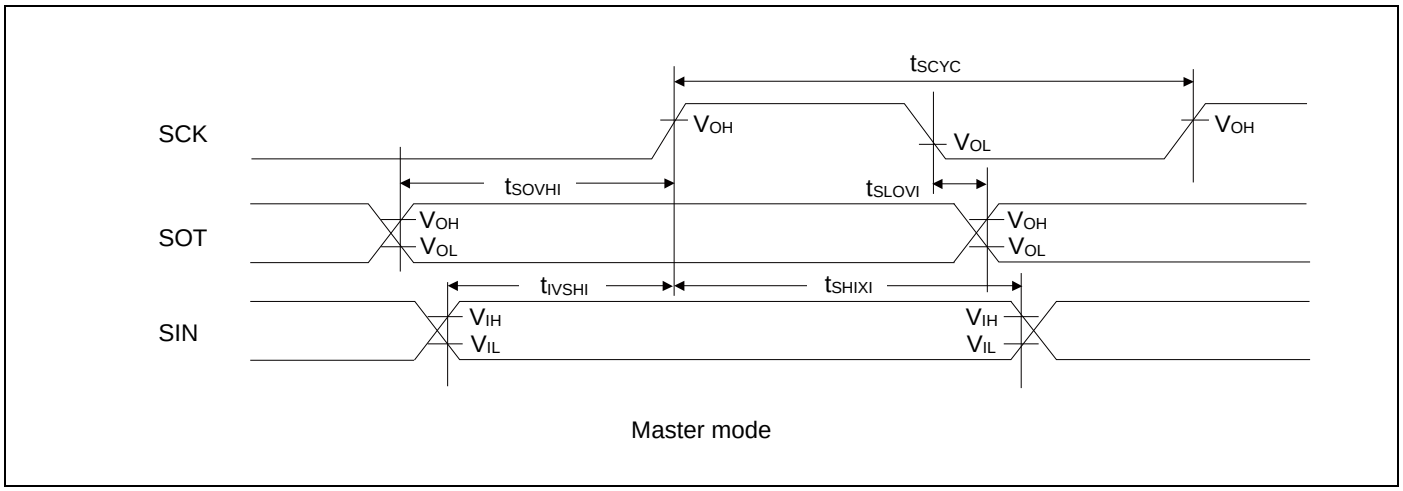
CSIO (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

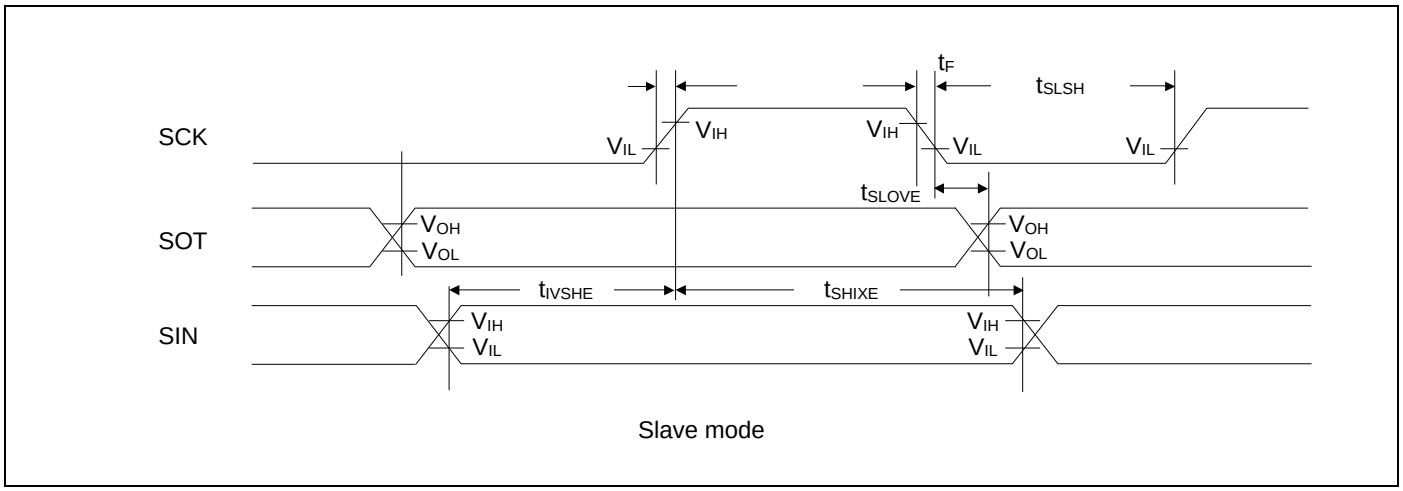
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to clock synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function Serial is connected to, see Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
- *For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*



Master mode

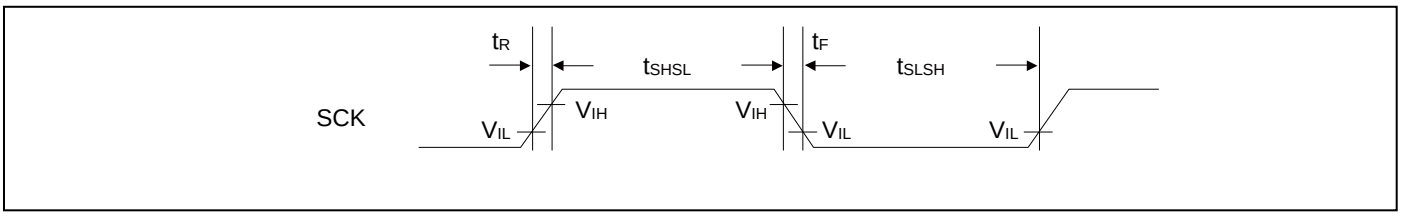


Slave mode

UART external clock input (EXT = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	t_F		-	5	ns	
SCK rising time	t_R		-	5	ns	



12.4.10 External Input Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

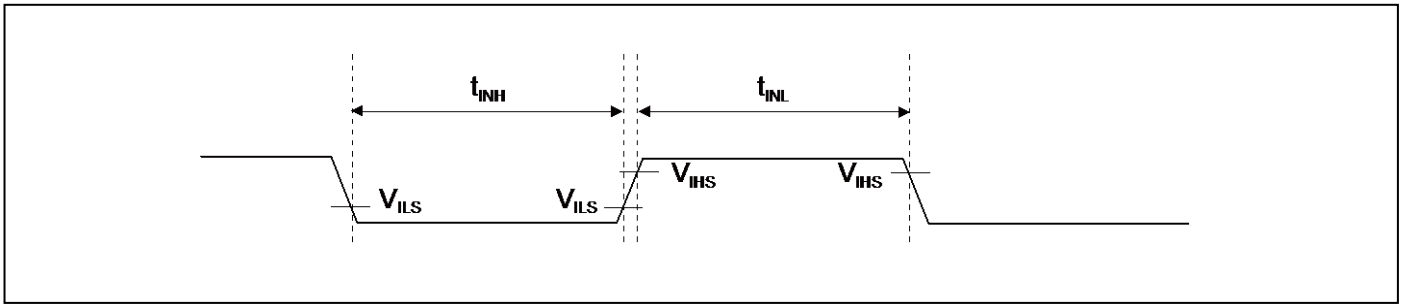
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	FRCKx	-	$2t_{CYCP}$*1	-	ns	Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*1	-	ns	Wave form generator
		INTxx, NMIX	*2	$2t_{CYCP}$ + 100*1	-	ns	External interrupt, NMI
			*3	500	-	ns	

*1: t_{CYCP} indicates the APB bus clock cycle time.

About the APB bus number which, Multi-function Timer, External interrupt is connected to, see Block Diagram in this data sheet.

*2: When in Run mode, in Sleep mode.

*3: When in Stop mode, in RTC mode, in Timer mode.



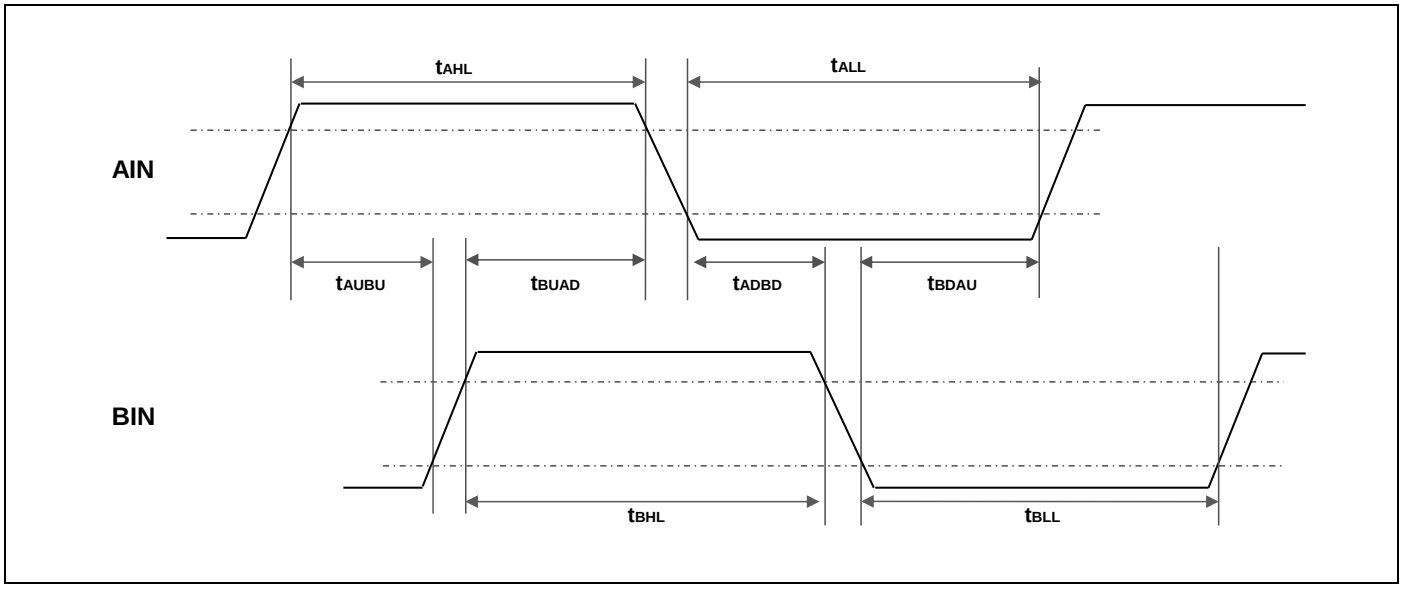
12.4.11 Quadrature Position/Revolution Counter Timing

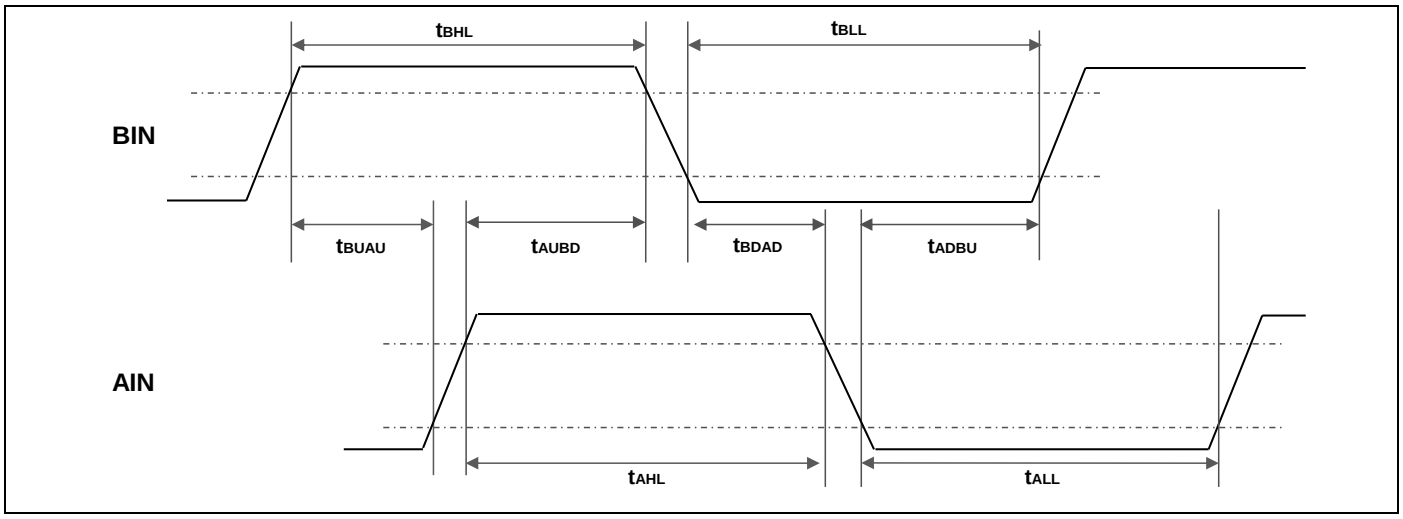
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

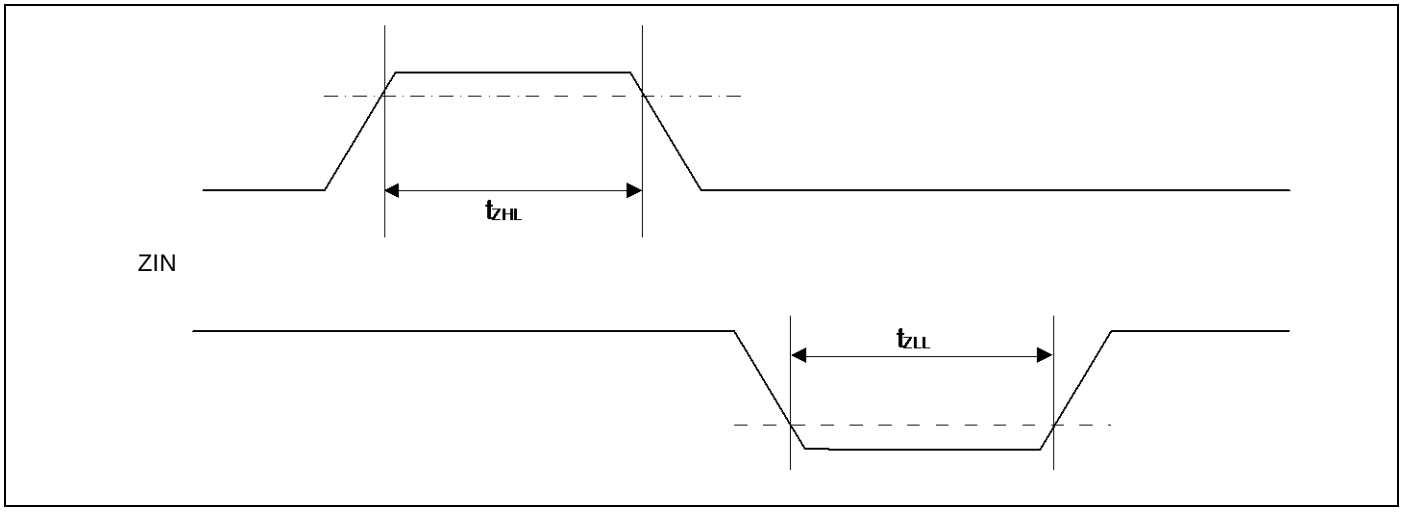
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t_{AHL}	-	$2t_{CYCP}$*	-	ns
AIN pin L width	t_{ALL}	-			
BIN pin H width	t_{BHL}	-			
BIN pin L width	t_{BLL}	-			
Time from AIN pin H level to BIN rise	t_{AUBU}	PC_Mode2 or PC_Mode3			
Time from BIN pin H level to AIN fall	t_{BUAD}	PC_Mode2 or PC_Mode3			
Time from AIN pin L level to BIN fall	t_{ADBD}	PC_Mode2 or PC_Mode3			
Time from BIN pin L level to AIN rise	t_{BDAU}	PC_Mode2 or PC_Mode3			
Time from BIN pin H level to AIN rise	t_{BUAU}	PC_Mode2 or PC_Mode3			
Time from AIN pin H level to BIN fall	t_{AUBD}	PC_Mode2 or PC_Mode3			
Time from BIN pin L level to AIN fall	t_{BDAD}	PC_Mode2 or PC_Mode3			
Time from AIN pin L level to BIN rise	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin H width	t_{ZHL}	QCR:CGSC=0			
ZIN pin L width	t_{ZLL}	QCR:CGSC=0			
Time from determined ZIN level to AIN/BIN rise and fall	t_{ZABE}	QCR:CGSC=1			
Time from AIN/BIN rise and fall time to determined ZIN level	t_{ABEZ}	QCR:CGSC=1			

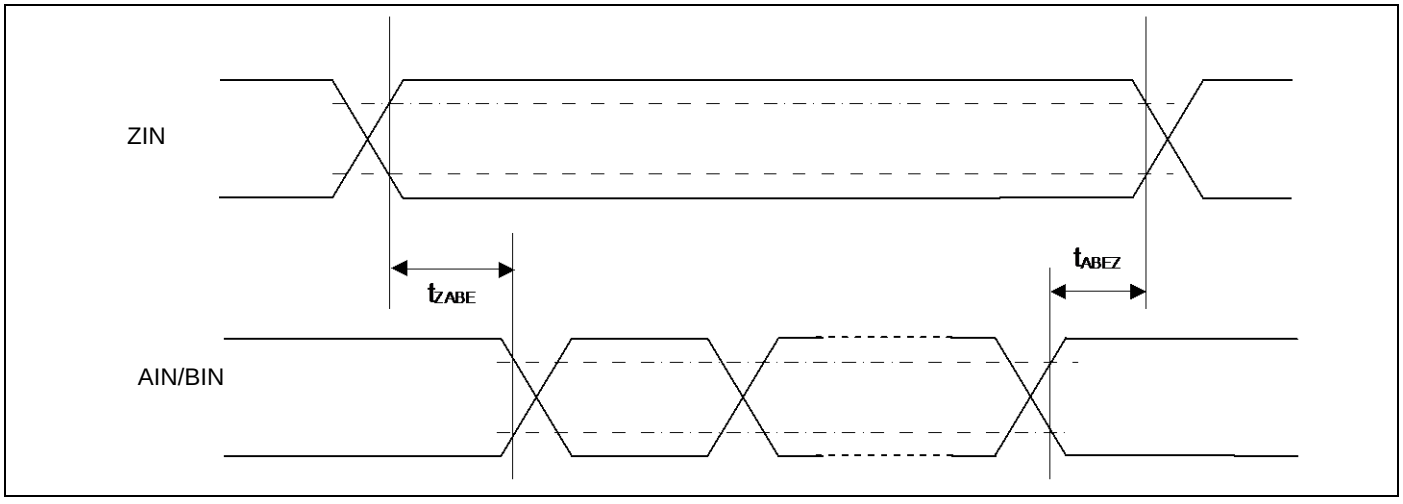
*: t_{CYCP} indicates the APB bus clock cycle time.

About the APB bus number which Quadrature Position/Revolution Counter is connected to, see Block Diagram in this data sheet.




tBHL
tBLL
BIN
tBUAU
tAUBD
tBDAD
tADBU
AIN
tAHL
tALL


tZHL
ZIN
tZLL


ZIN
tZABE
tABEZ
AIN/BIN

12.4.12 I²C Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

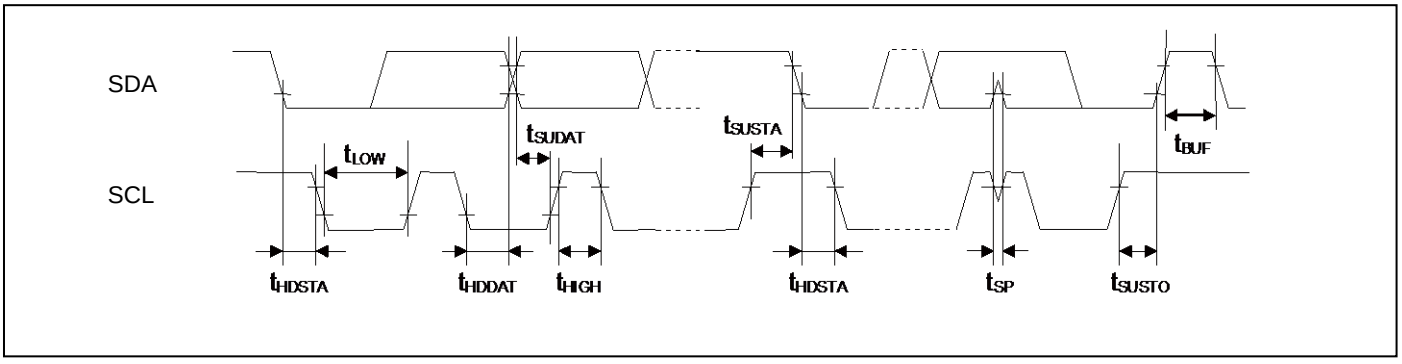
Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock L width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock H width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) Start condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between Stop condition and Start condition	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively.
Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it doesn't extend at least L period (t_{LOW}) of device's SCL signal.

*3: A Fast-mode I²C bus device can be used on a Standard-mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I²C is connected to, see Block Diagram in this data sheet.
To use Standard-mode, set the APB bus clock at 2 MHz or more.
To use Fast-mode, set the APB bus clock at 8 MHz or more.



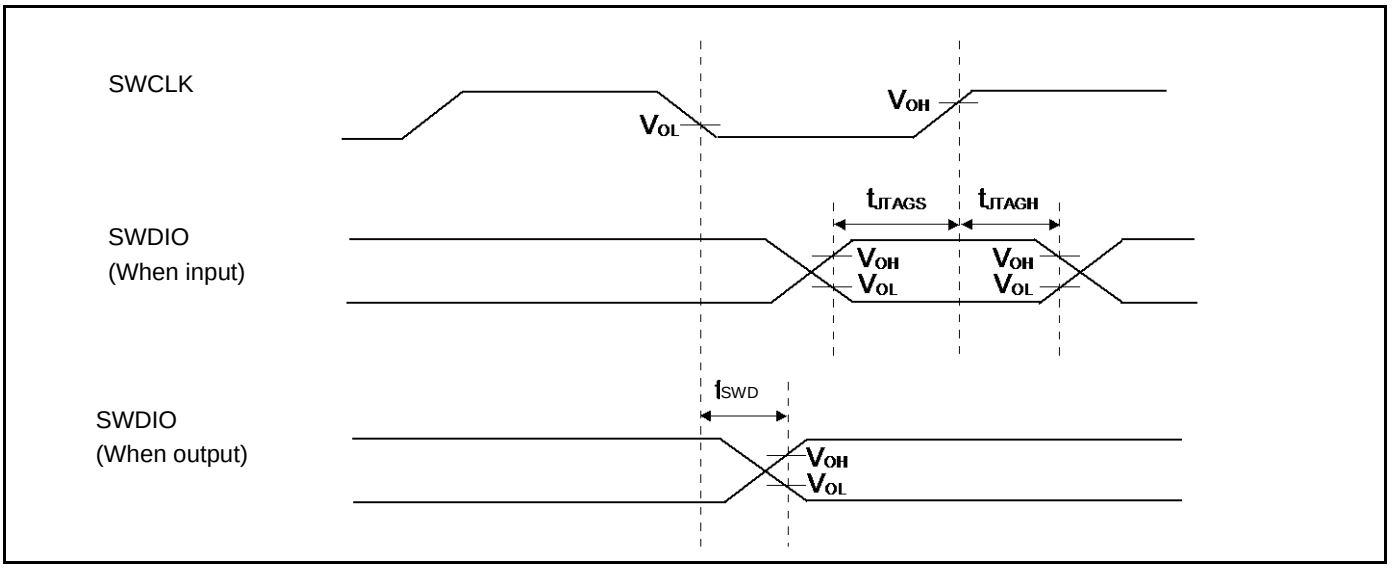
12.4.13 SWD Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SWDIO setup time	t_{SWS}	SWCLK, SWDIO	-	15	-	ns	
SWDIO hold time	t_{SWH}	SWCLK, SWDIO	-	15	-	ns	
SWDIO delay time	t_{SWD}	SWCLK, SWDIO	-	-	45	ns	

Note:

- *When the external load capacitance C_L = 30 pF.*



12.5 12-bit A/D Converter

Electrical characteristics for the A/D converter

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-	± 3.0	± 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential Nonlinearity	-	-	-	± 2.5	± 3.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-	± 15	± 20	mV	
Full-scale transition voltage	V_{FST}	ANxx	-	AVRH ± 15	AVRH ± 20	mV	
Conversion time	-	-	1.0*1	-	-	µs	
Sampling time*2	t_S	-	0.3	-	10	µs	
Compare clock cycle*3	t_{CCK}	-	50	-	1000	ns	
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Analog input capacity	C_{AIN}	-	-	-	9.7	pF	
Analog input resistance	R_{AIN}	-	-	-	1.5	kΩ	V_{CC} ≥ 4.5 V
					2.2		V_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AVRL	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	V_{CC}	V	
		AVRL	V_{SS}	-	V_{SS}	V	

*1: Conversion time is the value of sampling time (t_S) + compare time (t_C).

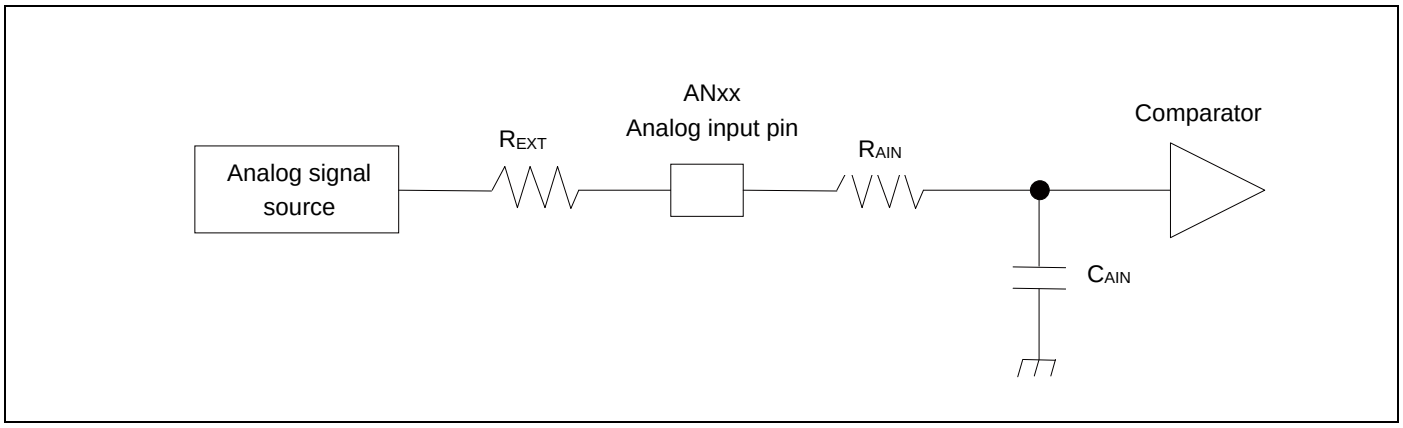
The condition of the minimum conversion time is when the value of sampling time: 300 ns, the value of sampling time: 700 ns. Ensure that it satisfies the value of sampling time (t_S) and compare clock cycle (t_{CCK}).
For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM3 Family Peripheral Manual Analog Macro Part.

The register settings of the A/D Converter are reflected in the operation according to the APB bus clock timing.
For the number of the APB bus to which the A/D Converter is connected, see Block Diagram.
The base clock (HCLK) is used to generate the sampling time and the compare clock cycle.

*2: A necessary sampling time changes by external impedance.

Ensure that it set the sampling time to satisfy (Equation 1).

*3: Compare time (t_C) is the value of (Equation 2).



(Equation 1) $t_S \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN}: Input resistance of A/D = 1.5 kΩ at 4.5 V ≤ V_{CC} ≤ 5.5 V
Input resistance of A/D = 2.2 kΩ at 2.7 V ≤ V_{CC} < 4.5 V

C_{AIN}: Input capacity of A/D = 9.7 pF at 2.7 V ≤ V_{CC} ≤ 5.5 V

R_{EXT}: Output impedance of external circuit

(Equation 2) $t_C = t_{CCK} \times 14$

t_C: Compare time

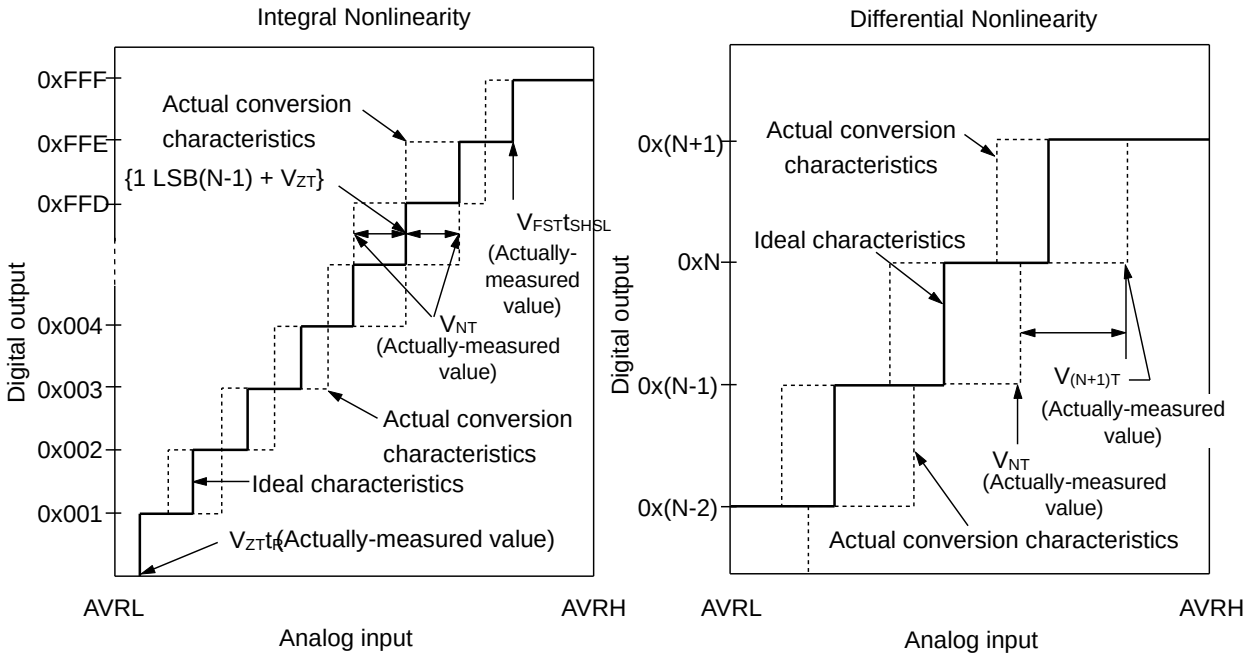
t_{CCK}: Compare clock cycle

Definition of 12-bit A/D Converter Terms

■Resolution: Analog variation that is recognized by an A/D converter.

■Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.

■Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.

V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.

V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.

V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

12.6 Low-Voltage Detection Characteristics

12.6.1 Low-Voltage Detection Reset

(T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHR[*1] = 00000	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH		2.30	2.50	2.70	V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00001	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00010	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	8160 × t_{CYCP}[*2]	µs	
LVD detection delay time	t_{LVDDL}	-	-	-	200	µs	

*1: SVHR bit of Low-Voltage Detection Voltage Control Register (LVD_CTL) is reset to SVHR = 00000 by low voltage detection reset.

*2: t_{CYCP} indicates the APB2 bus clock cycle time.

12.6.2 Interrupt of Low-Voltage Detection

(T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI = 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		3.04	3.30	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		3.40	3.70	4.00	V	When voltage rises
Detected voltage	VDL	SVHI = 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		3.50	3.80	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.10	4.43	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		3.86	4.20	4.54	V	When voltage rises
Detected voltage	VDL	SVHI = 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		3.96	4.30	4.64	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	8160 × t_{CYCP}*	µs	
LVD detection delay time	t_{LVDDL}	-	-	-	200	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

12.7 Flash Memory Write/Erase Characteristics

12.7.1 Write / Erase time

(VCC = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

Parameter	Value		Unit	Remarks
	Typ	Max		
Sector erase time	0.3	0.7	s	Includes write time prior to internal erase
Half word (16-bit) write time	16	282	µs	Not including system-level overhead time
Chip erase time	2.4	5.6	s	Includes write time prior to internal erase

*: The typical value is immediately after shipment, the maximum value is guarantee value under 10,000 cycle of erase/write.

12.7.2 Write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	

*: At average + 85°C

12.8 Return Time from Low-Power Consumption Mode

12.8.1 Return Factor: Interrupt

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

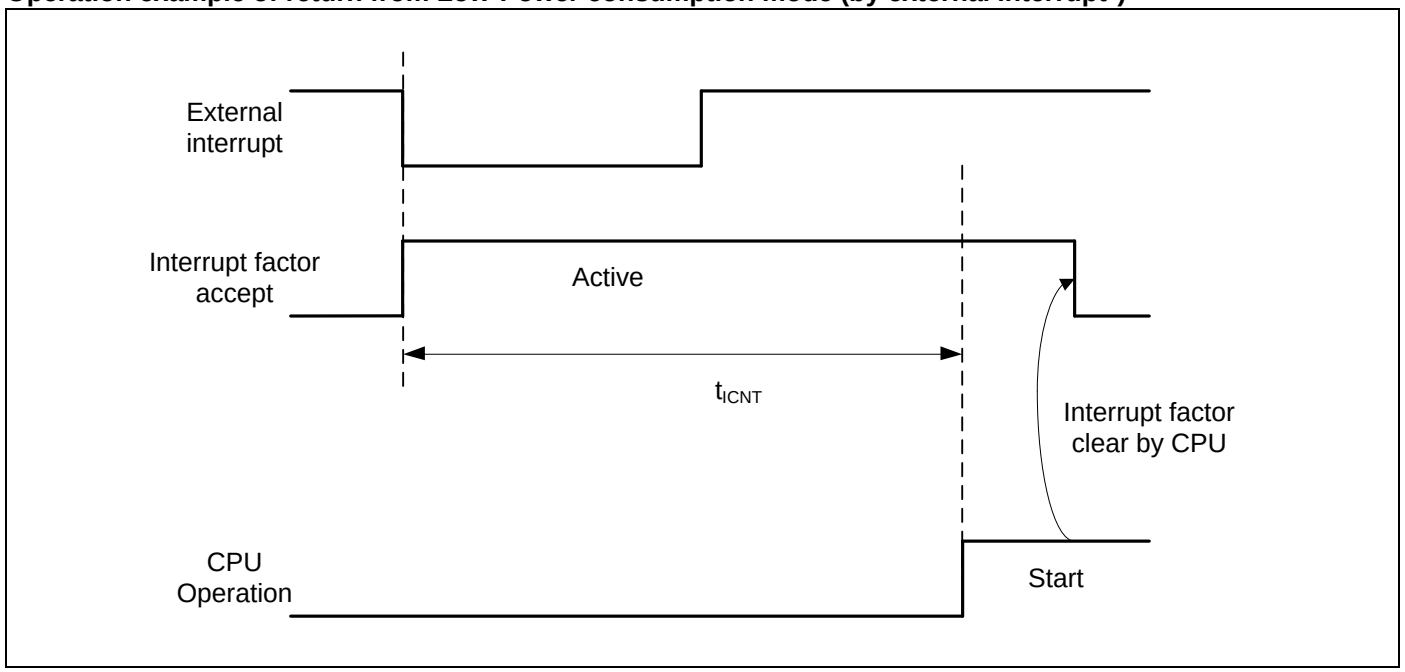
Return Count Time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{ICNT}	t_{CYCC}		µs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		43	83	µs	
Low-speed CR Timer mode		310	620	µs	
Sub Timer mode		534	724	µs	
RTC mode, Stop mode		278	479	µs	

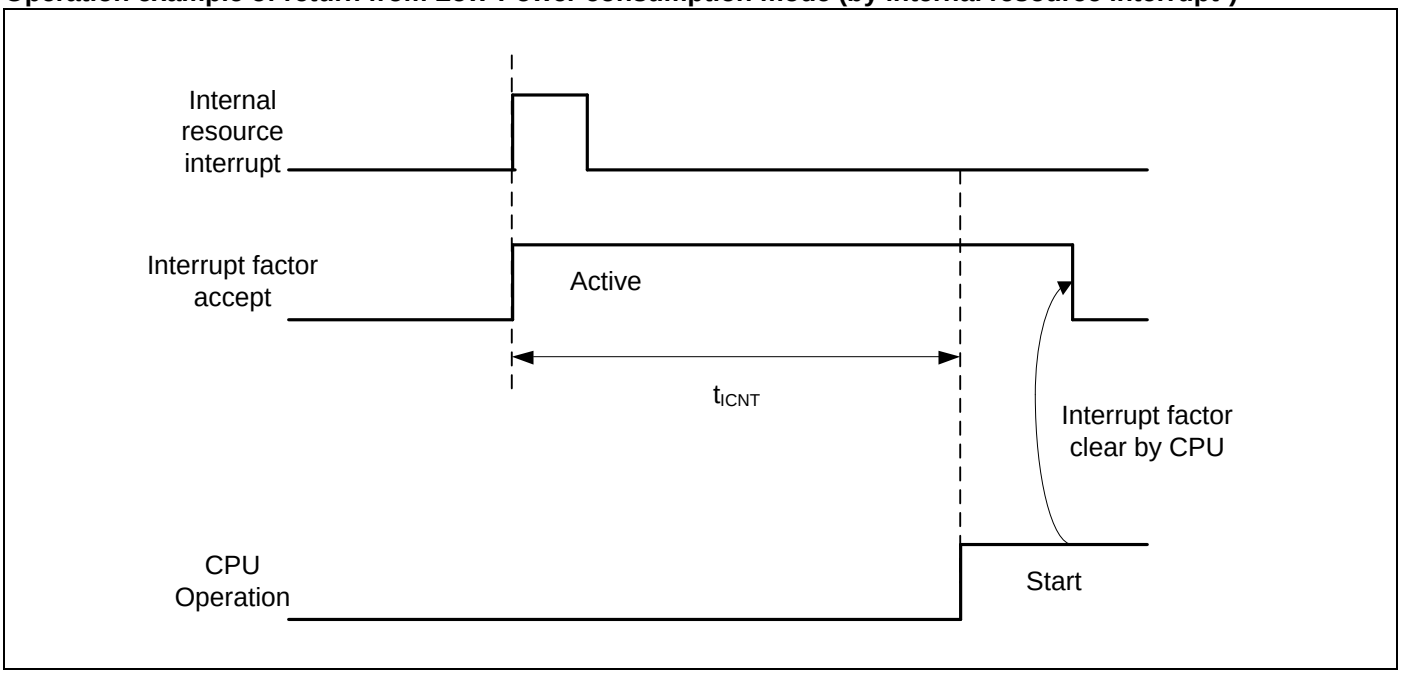
*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by external interrupt*)



*: External interrupt is set to detecting fall edge.

Operation example of return from Low-Power consumption mode (by internal resource interrupt*)



*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
- *See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM3 Family Peripheral Manual.*
- *When interrupt recoveries, the operation mode that CPU recoveries depend on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in FM3 Family Peripheral Manual.*

12.8.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

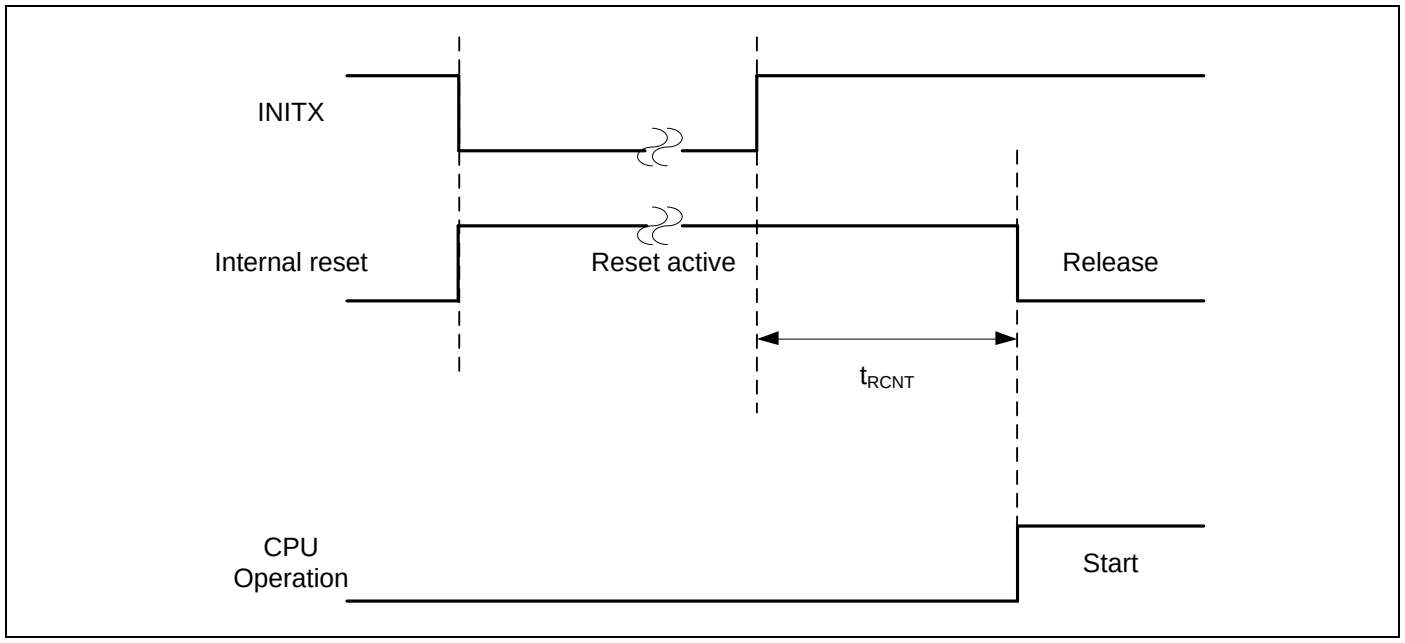
Return Count Time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

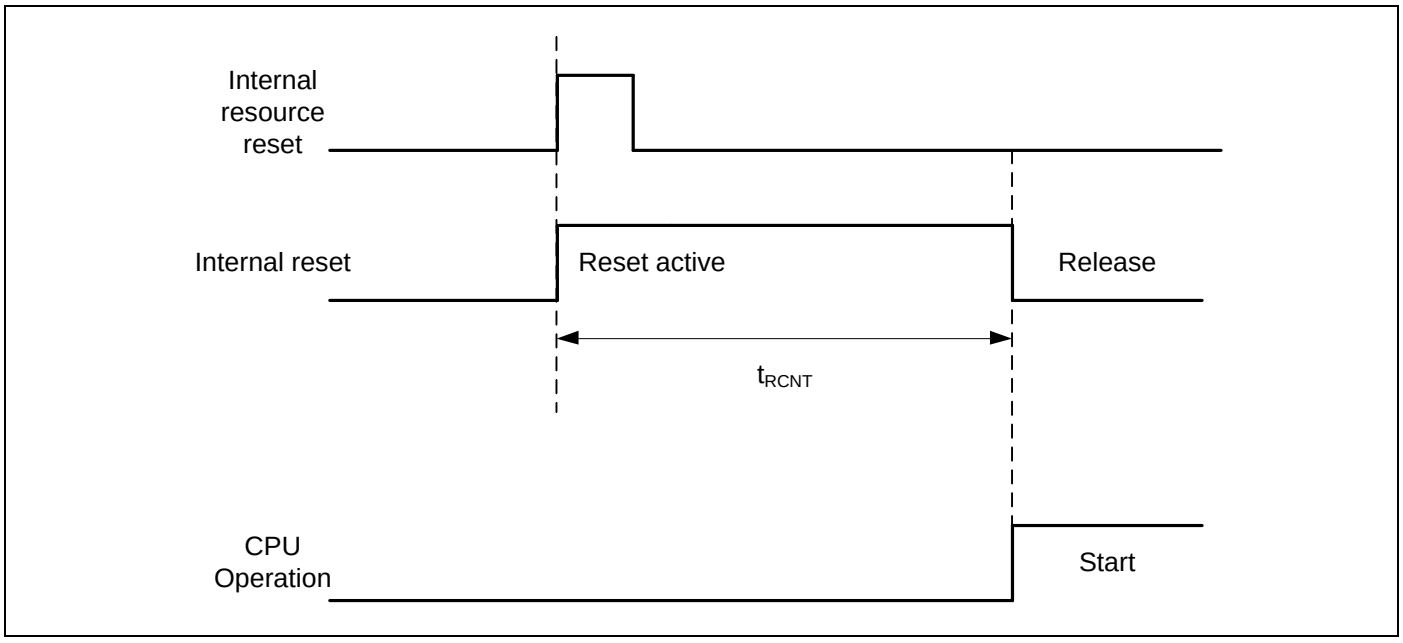
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	149	264	µs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		149	264	µs	
Low-speed CR Timer mode		318	603	µs	
Sub Timer mode		308	583	µs	
RTC mode, Stop mode		248	443	µs	

*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by INITX)



Operation example of return from low power consumption mode (by internal resource reset*)



*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

Notes:

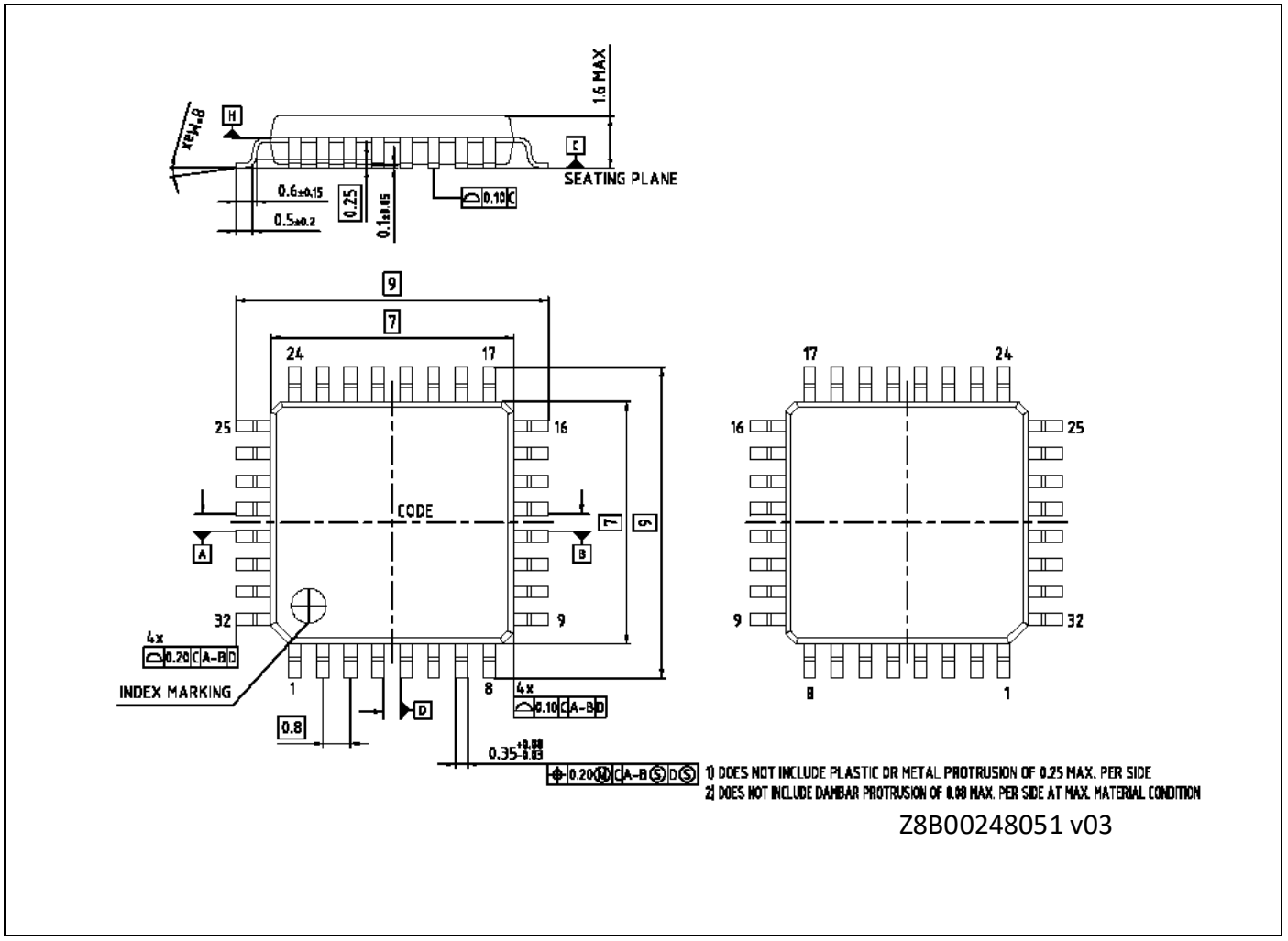
- *The return factor is different in each Low-Power consumption modes.*
- *See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM3 Family Peripheral Manual.*
- *When interrupt recoveries, the operation mode that CPU recoveries depend on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in FM3 Family Peripheral Manual.*
- *The time during the power-on reset/low-voltage detection reset is excluded. See Power-on Reset Timing in AC Characteristics in Electrical Characteristics for the detail on the time during the power-on reset/low -voltage detection reset.*
- *When in recovery from reset, CPU changes to the High-speed CR Run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the Main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

13. Ordering Information

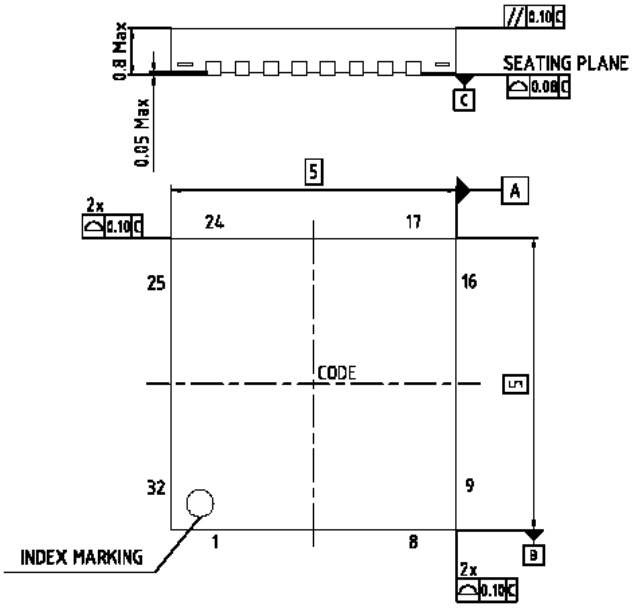
Part number	Package
CY9BF121JPMC-G-JNE2	Plastic・LQFP32 (0.8 mm pitch), 32 pin (LQB032)
CY9BF121JWQN-G-JNE2	Plastic・QFN32 (0.5 mm pitch), 32 pin (WNU032)

14. Package Dimensions

Package Type	Package Code
LQFP 32	LQB032



Package Type	Package Code
QFN 32	WNU032



1) MAX. PACKAGE WARPAGE IS 0.05
2) MAXIMUM ALLOWABLE BURRS IS 0.076 IN ALL DIRECTIONS

Z8B00249000 v03

15. Major Changes

Spansion Publication Number: DS706-00053

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 1.0		
-	-	Preliminary → Data Sheet
-	-	Company name and layout design change
2	Features	Revised I^2C operation mode name
4	Features	Revised Channel number of MFT A/D activation compare
6	Product Lineup	・Revised channel number of MFT A/D activation compare ・Added notes of Built-in high speed CR accuracy
7	Packages	Corrected Package code
9	Pin Assignment	Corrected Package code
20	I/O Circuit Type	Corrected the remarks of type E and F
29	Block Diagram	Revised Channel number of MFT A/D activation compare
40,42	Electrical Characteristics 3.Dc Characteristics(1) Current Rating	Revised the values of “TBD”
48	Electrical Characteristics 3.Ac Characteristics(6)Power-On Reset Timing	Revised the values of “TBD”
61	Electrical Characteristics 3.Ac Characteristics(11) I^2c Timing	・Revised I^2C operation mode name ・Revised the value of noise filter ・Revised the notes explanation
62	Electrical Characteristics 3.Ac Characteristics(12) Swd Timing	Added the value of SWDIO delay time
63	Electrical Characteristics 5. 12-Bit A/D Converter Electrical Characteristics	・Added the value of sampling time ・Revised the notes explanation ・Revised the value of Differential Nonlinearity +/-2.5LSB →+/-3.5LSB ・Deleted (Preliminary value) description
68	Electrical Characteristics 7. Flash Memory Write/Erase Characteristics	・Revised the values of “TBD” ・Revised the notes of Erase/write cycles and data hold time ・Deleted (target value) description
69,71	Electrical Characteristics 8. Return Time From Low-Power Consumption Mode	Revised the values of “TBD”
75	Package Dimensions	Corrected Package code
Revision 2.0		
20	I/O Circuit Type	Added about +B input
31	Memory Map · Memory Map(2)	Added the summary of Flash memory sector and the note
38, 39	Electrical Characteristics 1. Absolute Maximum Ratings	· Added the Clamp maximum current · Added about +B input
40	Electrical Characteristics 2. Recommended Operation Conditions	Added the note about less than the minimum power supply voltage
41, 42	Electrical Characteristics 3. DC Characteristics (1) Current Rating	· Changed the table format · Added Main Timer mode current
47	Electrical Characteristics 4. AC Characteristics (4-1) Operating Conditions Of Main PLL (4-2) Operating Conditions Of Main PLL	Added the figure of Main PLL connection
48	Electrical Characteristics 4. AC Characteristics (6) Power-On Reset Timing	Changed the figure of timing

Page	Section	Change Results
50-57	Electrical Characteristics 4. Ac Characteristics (8) Csio/Uart Timing	· Modified from UART Timing to CSIO/UART Timing · Changed from Internal shift clock operation to Master mode · Changed from External shift clock operation to Slave mode
63	Electrical Characteristics 5. 12bit A/D Converter	Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage
73	Ordering Information	Changed notation of part number

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: CY9B120J Series 32-bit ARM® Cortex®-M3 FM3 Microcontroller
Document Number: 002-05657

Revision	ECN	Submission Date	Description of Change
**	–	03/31/2015	Migrated to Cypress and assigned document number 002-05657. No change to document contents or format.
*A	5167951	03/14/2016	Updated to Cypress format.
*B	5543718	03/08/2017	"Modified RTC description in "Features, Real-Time Clock(RTC)" Changed starting count value from 01 to 00. Deleted "second , or day of the week" in the Interrupt function (Page 2) Updated "12.4.7 Power-On Reset Timing". Changed parameter from "Power Supply rising time(t_{VCCR})[ms]" to "Power ramp rate(dV/dt)[mV/us]" and added some comments (Page 46) Updated Package code and dimensions as follows (Page 7-9, 38, 71-73) FPT-32P-M30 -> LQB032, LCC-32P-M73 -> WNU032 Added the Baud rate spec in "12.5.10 CSIO/UART Timing"(Page 48, 50, 52, 54)
*C	5774756	06/20/2017	Adapted new Cypress logo
*D	8082013	10/21/2024	Updated Ordering Information. Changed MB into CY globally. Replaced the package diagram spec 002-13879 by Z8B00248051, 002-15907 by Z8B00249000. Completing ECN Sunset Review.

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